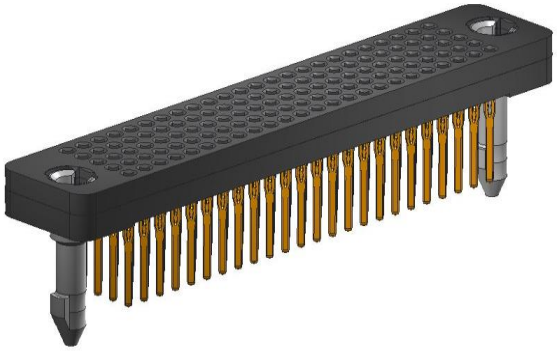
GT-17-131

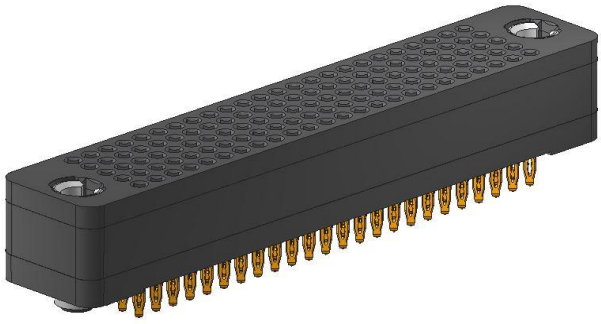
HD Stacker

High Speed Characterization Report for Differential Applications

GSTBL-120-.270-G1
Top Mounted Connector



GSTB-120-.095-G1
Bottom Mounted Connector



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Revision: D

Revision History

Rev	Date	Approved	Description
A	7/10/2017	G. Hunziker, L. Blackwell	Initial Release
B	11/27/2017	L. Blackwell	Added PCB Layout Guide Appendix, updated Appendix C
C	5/21/2018	L. Blackwell	Updated test differential pair nomenclature, updated eye pattern test equipment settings
D	1/8/2019	L. Blackwell	Updated recommended finished hole size from 28 mil to 29 mil

Table of Contents

1. Introduction

This document contains results from testing that was performed in order to evaluate the high-frequency electrical performance of the GSTB High Density Stacker Connector (HD Stacker Connector) in differential signaling applications. All measurements (except eye diagrams) were taken using an Agilent E5071C network analyzer with TDR option connected to SMA-launch test fixture PCBs designed specifically for this testing. This report outlines frequency domain performance metrics such as insertion loss (IL), return loss (RL) and crosstalk, as well as time-domain performance metrics including impedance and eye pattern.

2. Product Overview

The GTSB Stacker connector uses compliant pin technology for board-to-board stackable connections.

3. Test Configuration

Stackable test fixture PCBs utilizing edge-launch SMA connectors were designed for the high speed tests. The signal layer design layout is seen in Figure 1.

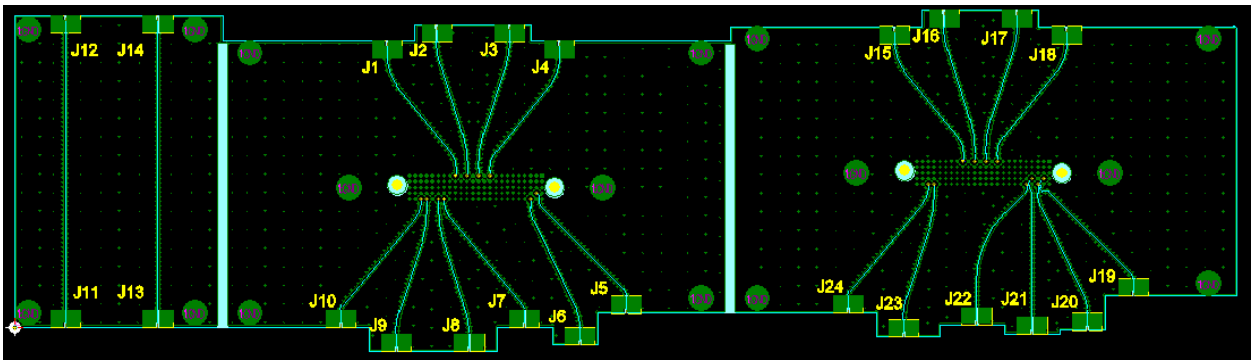


Figure 13. Test Fixture PCB layout

Top HD Stacker connectors (GSTBL-120-.270-G1) were pressed into one test PCB and bottom HD stacker connectors (GSTB-120-.095-G1) were pressed into a second test PCB. The test PCBs were stacked as shown in Figure 2.

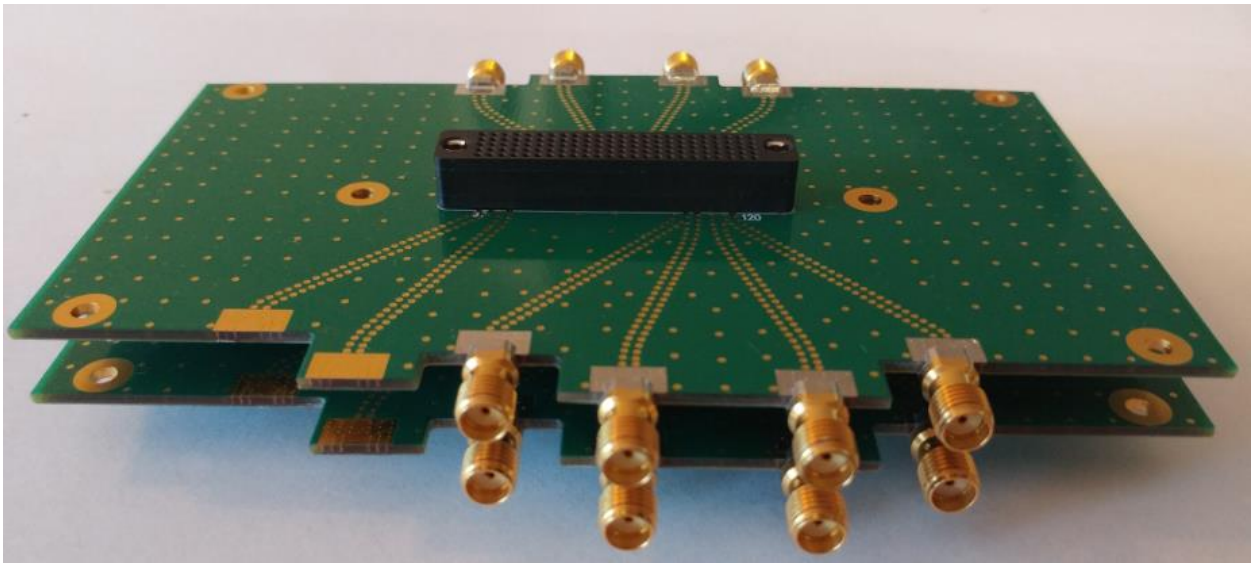
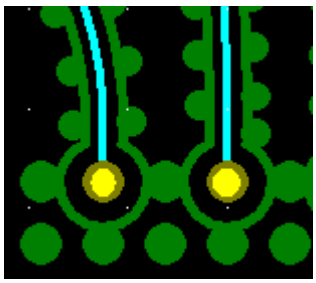
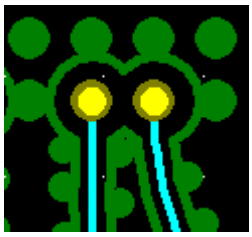
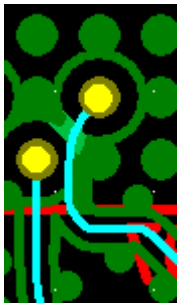


Figure 2. Stacked Test PCBs

Three differential pair configurations were tested:

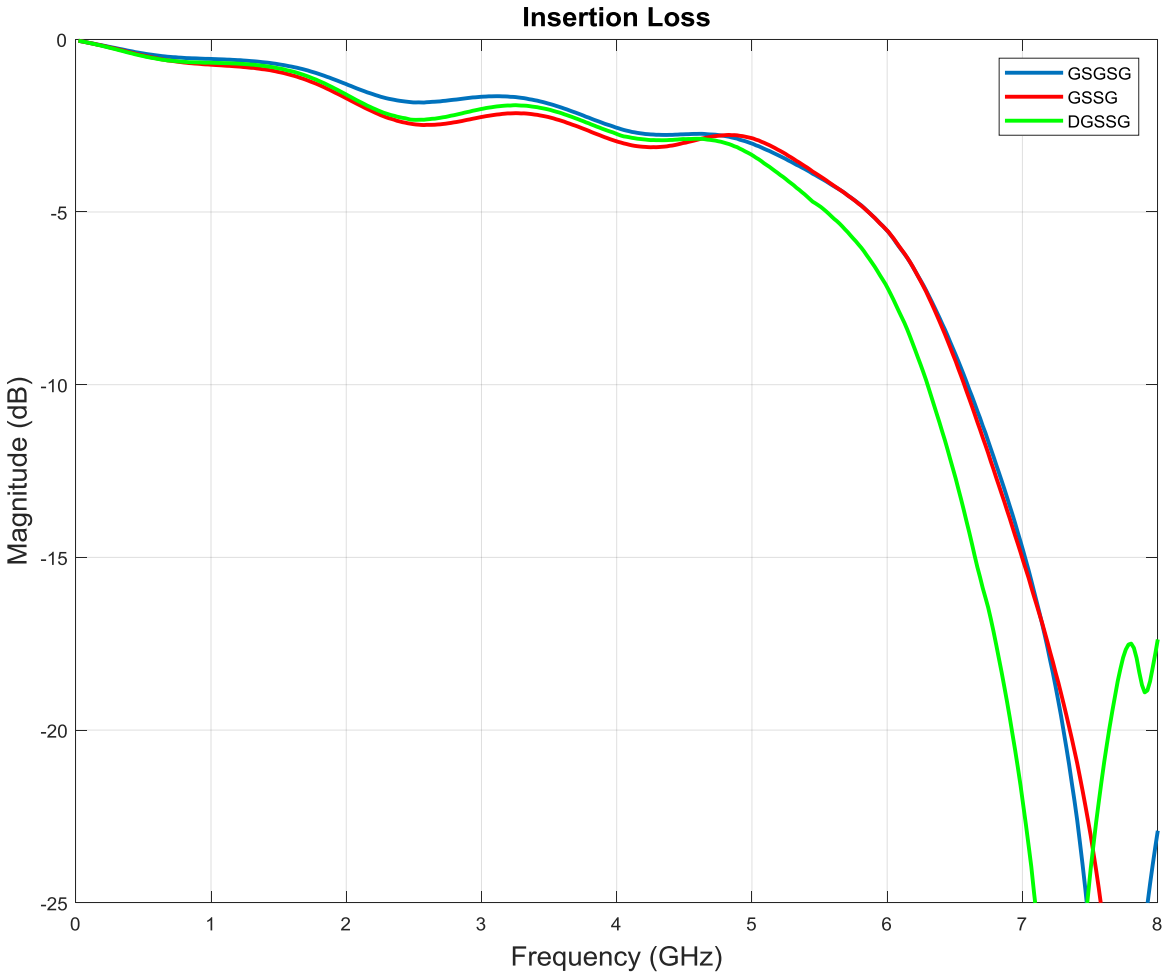
1. Signal-Ground-Signal (GSGSG)	2. Signal-Signal (GSSG)	3. Diagonal Signal-Signal (DGSSG)
		

4. Performance Summary

Test fixture PCB and test cabling loss have been de-embedded to show the performance of the stacked connector pair only.

4.1. Frequency Domain Analysis

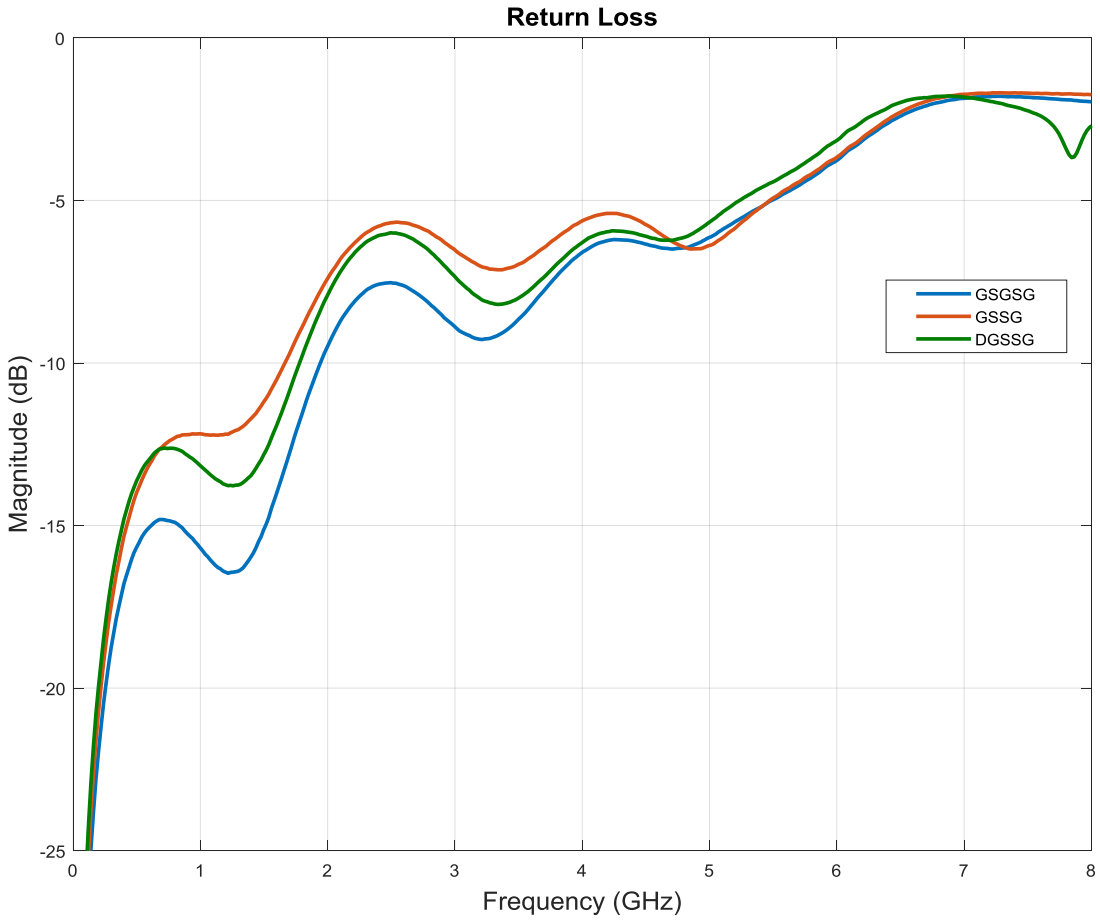
4.1.1. Insertion Loss



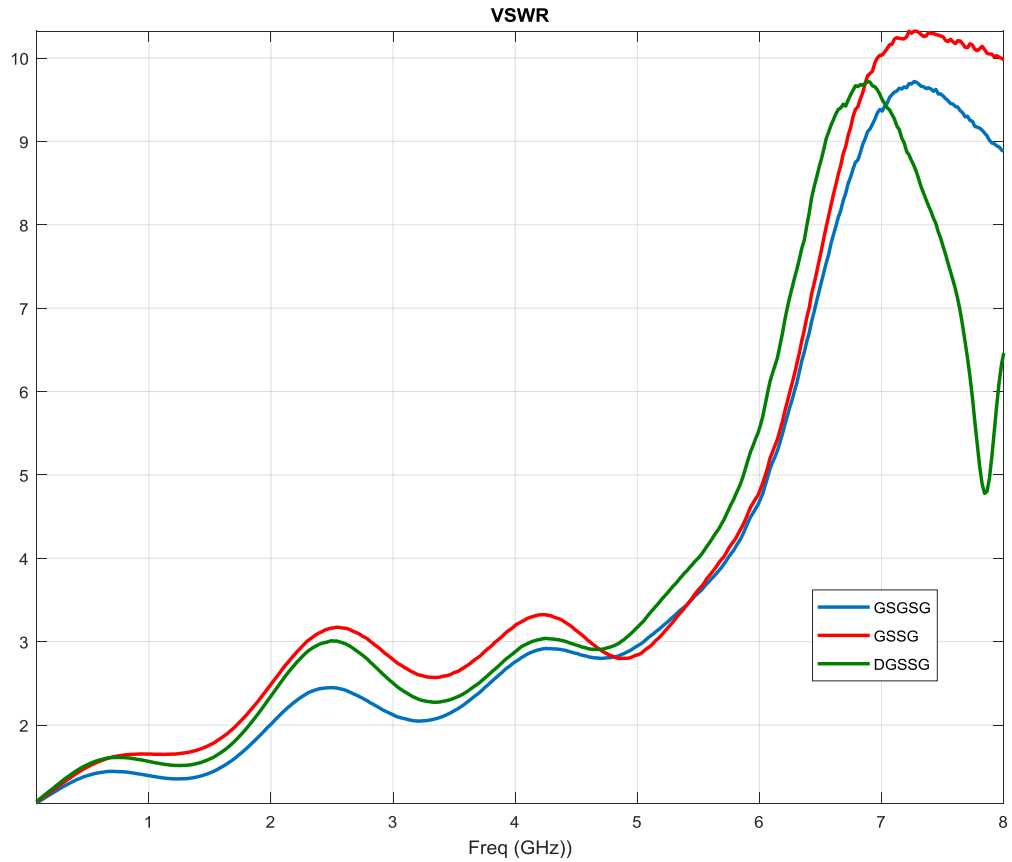
Parameter	Results
Insertion Loss	**-3dB @ 5.6GHz**
Electrical Bandwidth*	**12Gbps**

* The connector system electrical bandwidth is based on the -3dB insertion loss point of a single mated pair, rounded up to the nearest 0.5GHz to account for test system loss that could not be de-embedded from the results. The frequency is then doubled to determine an approximate data rate in gigabits per second (Gbps). For example, a connector with a -3 dB point of 2.3GHz would have a speed rating of 5.0Gbps.

4.1.2. Return Loss



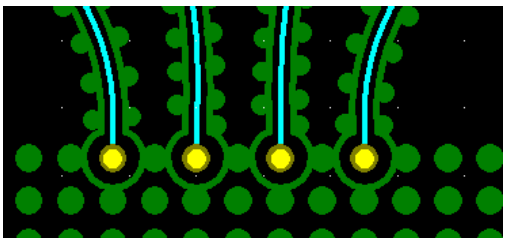
4.1.3. VSWR



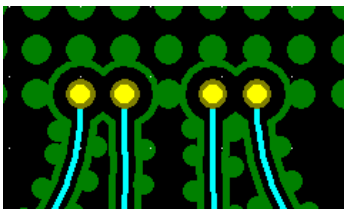
4.1.4. NEXT

Adjacent pairs of each configuration were tested to evaluate Near End Crosstalk:

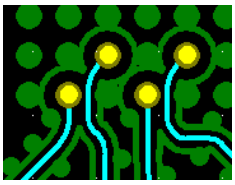
1. GSGSG

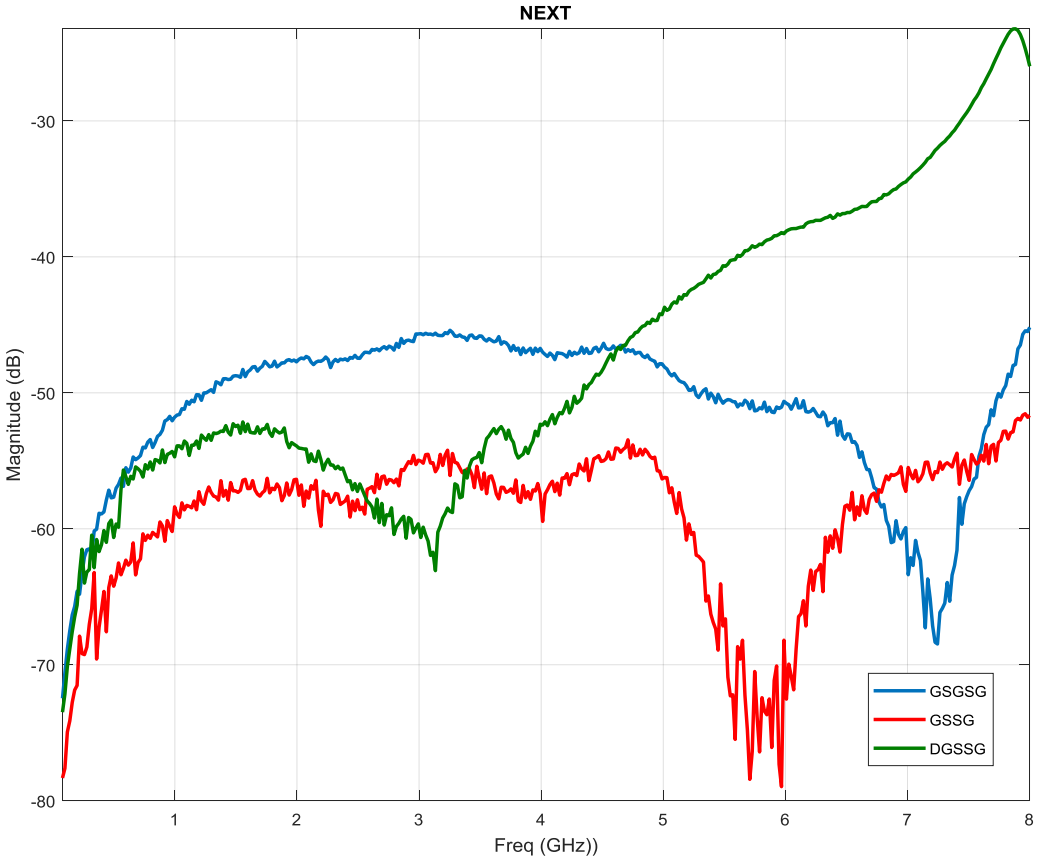


2. GSSG



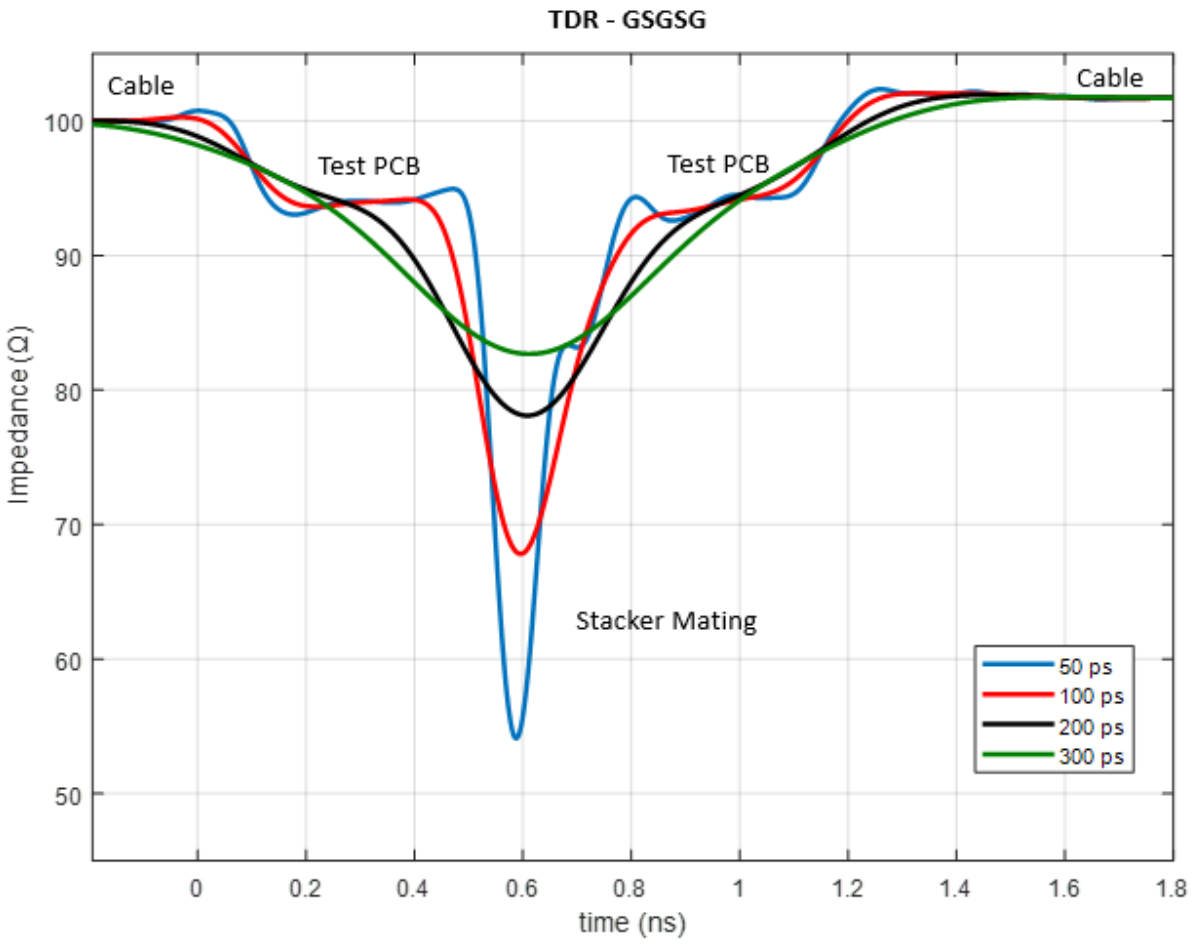
3. DGSSG

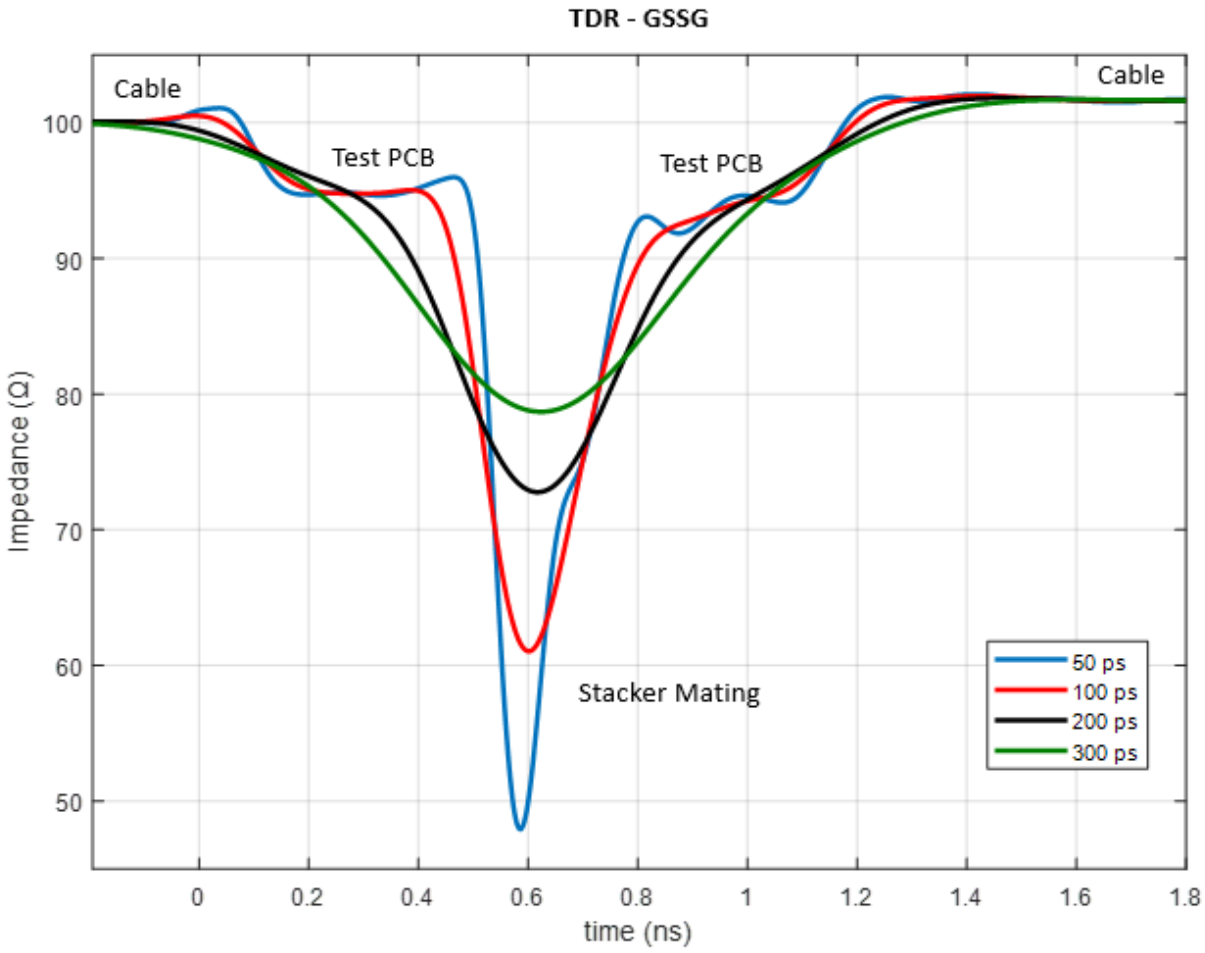


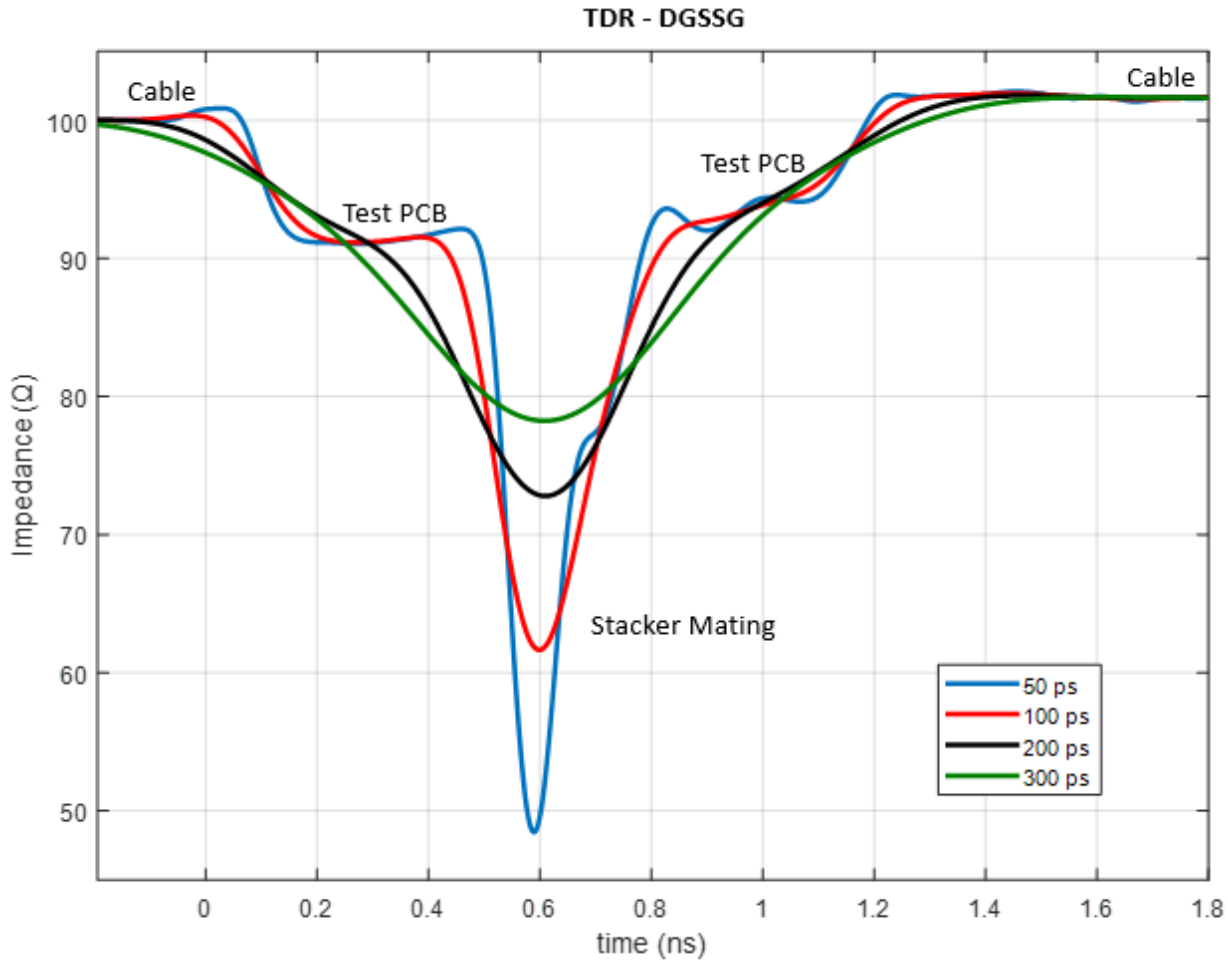


4.2 Time Domain Analysis

Time domain data was generated in real time by the Agilent Option TDR software package within the 5071C ENA network analyzer. Graphs for each GSGSG, GSSG, and DGSSG configurations are shown below for various rise times. Rise time is defined at 20% to 80% of the signal's rising edge.


TDR - GSGSG
Cable
Test PCB
Test PCB
Cable
Stacker Mating
50 ps
100 ps
200 ps
300 ps
Impedance (Ω)
time (ns)
100
90
80
70
60
50
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8





Eye Diagrams:

Eye pattern data was acquired using an Agilent N4901B Serial Bert and an Agilent Infiniium DCA-J 86100C Digital Communications Analyzer. A PRBS 2^7-1 waveform with a peak-to-peak voltage of 300mV was used. The rise time of the waveform was approximately 15ps. No equalization or filtering was used. Patterns for each GSGSG, GSSG, and DGSS G configurations are shown below for various bit rates.

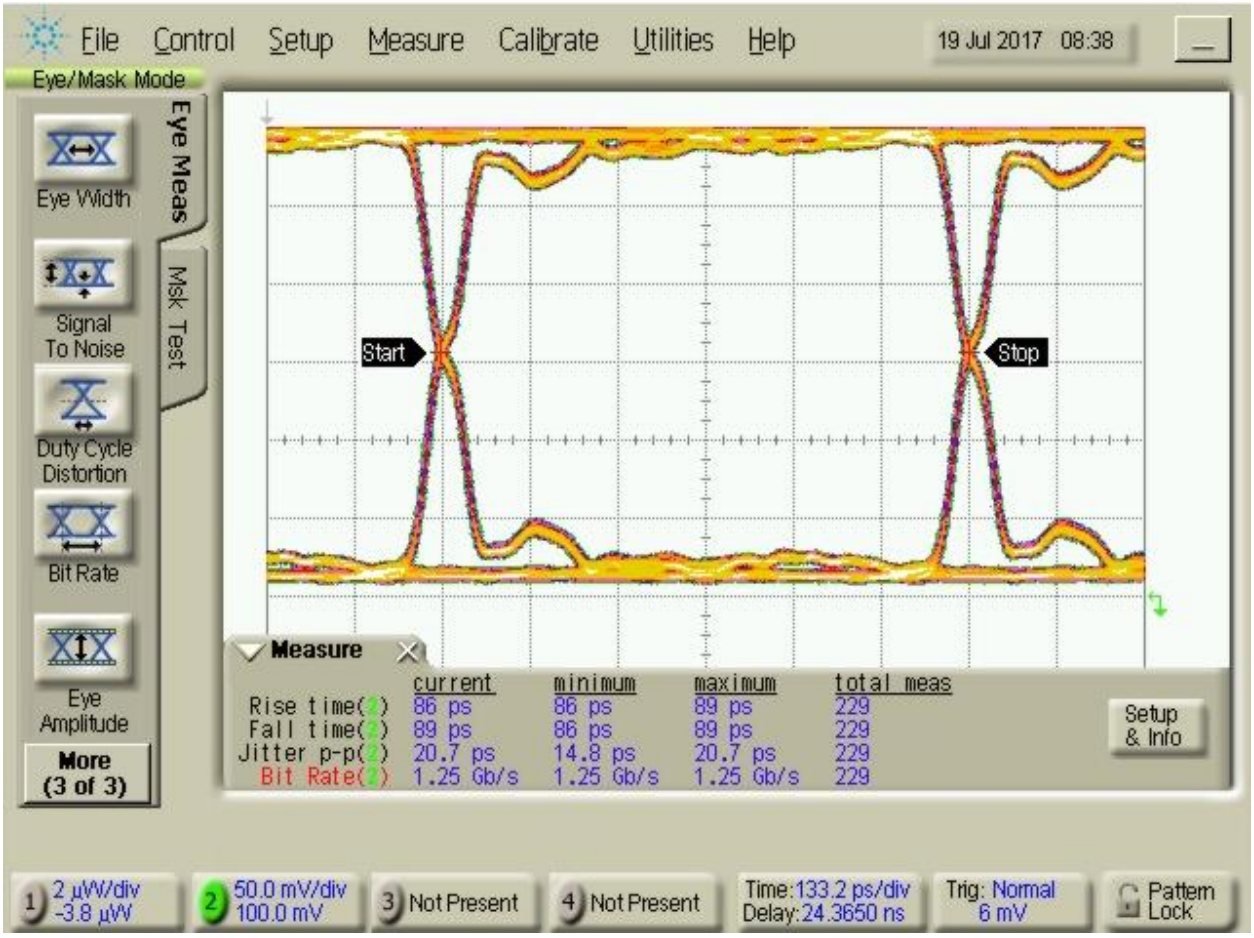


Figure 3: Eye diagram of GSGSG configuration at 1.25Gbps

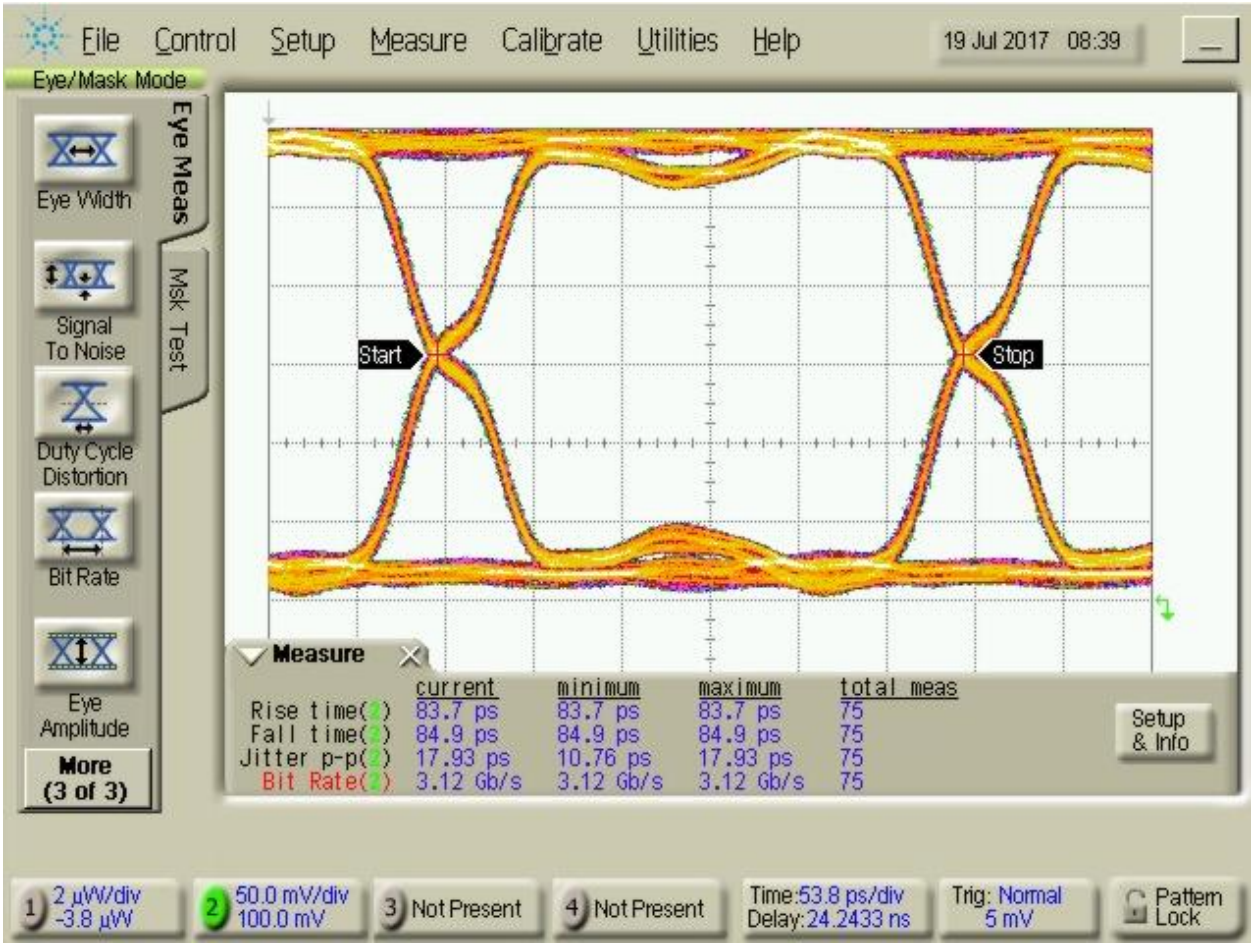


Figure 4: Eye diagram of GSGSG configuration at 3.125Gbps

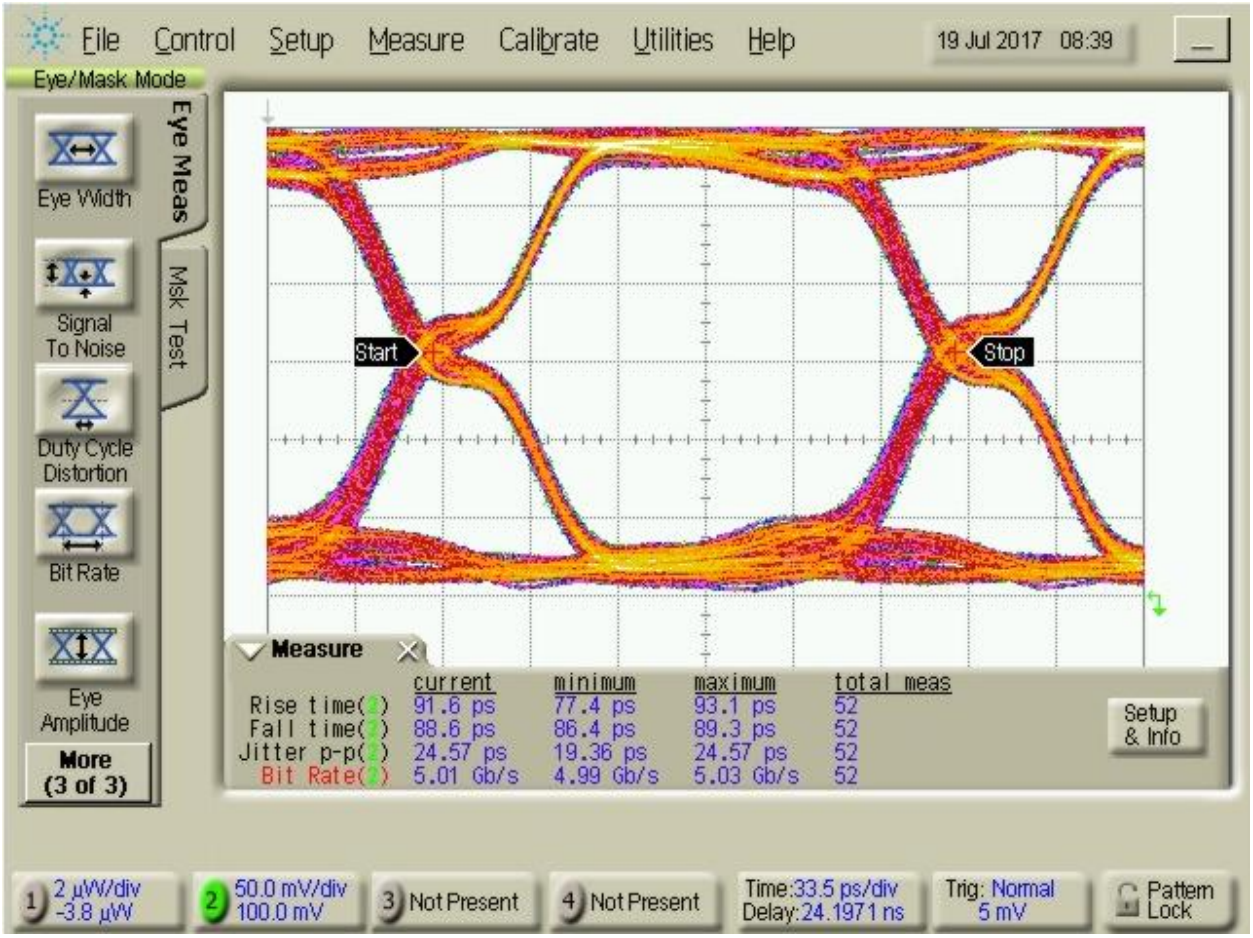


Figure 5: Eye diagram of GSGSG configuration at 5Gbps

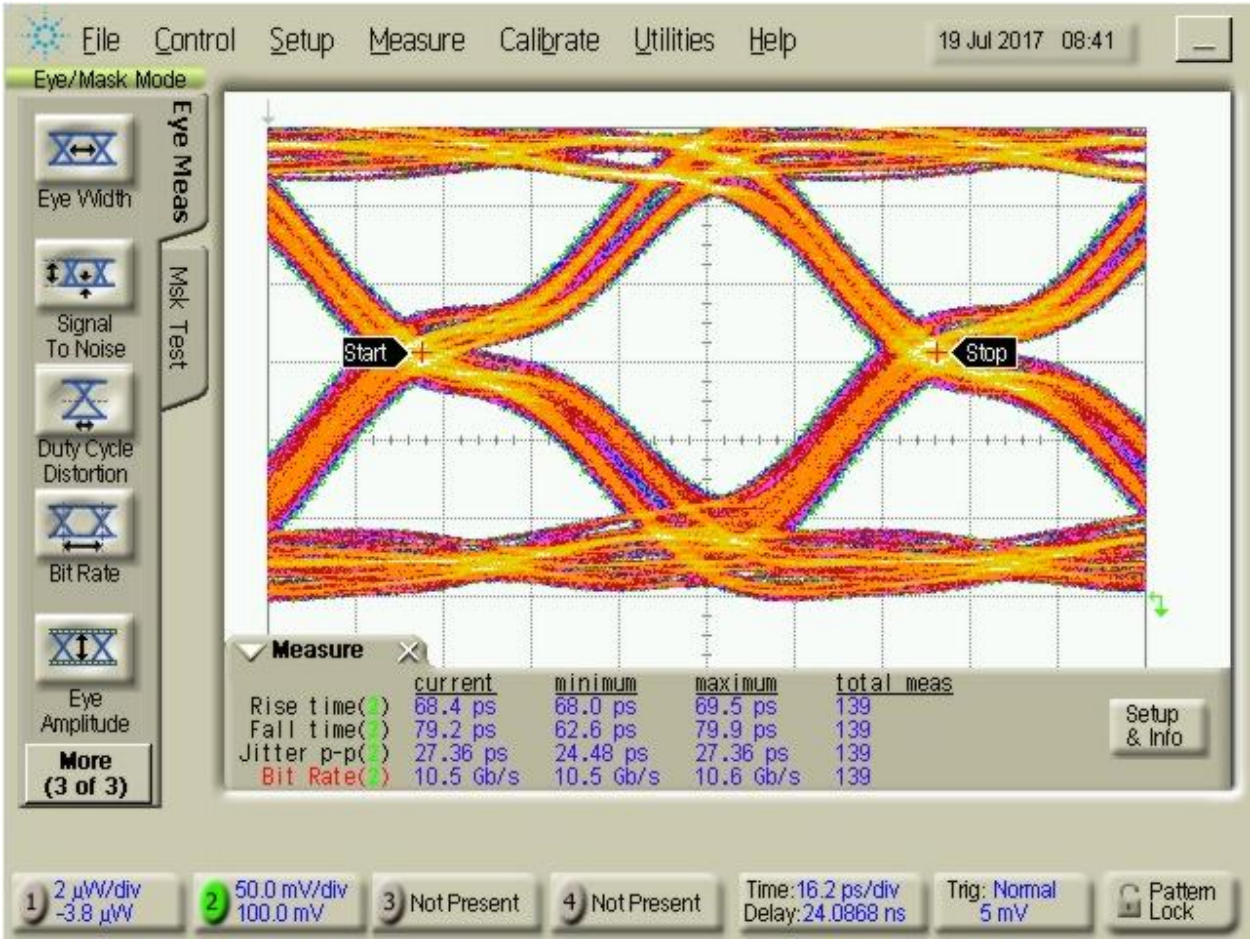


Figure 6: Eye diagram of GSGSG configuration at 10.3125Gbps

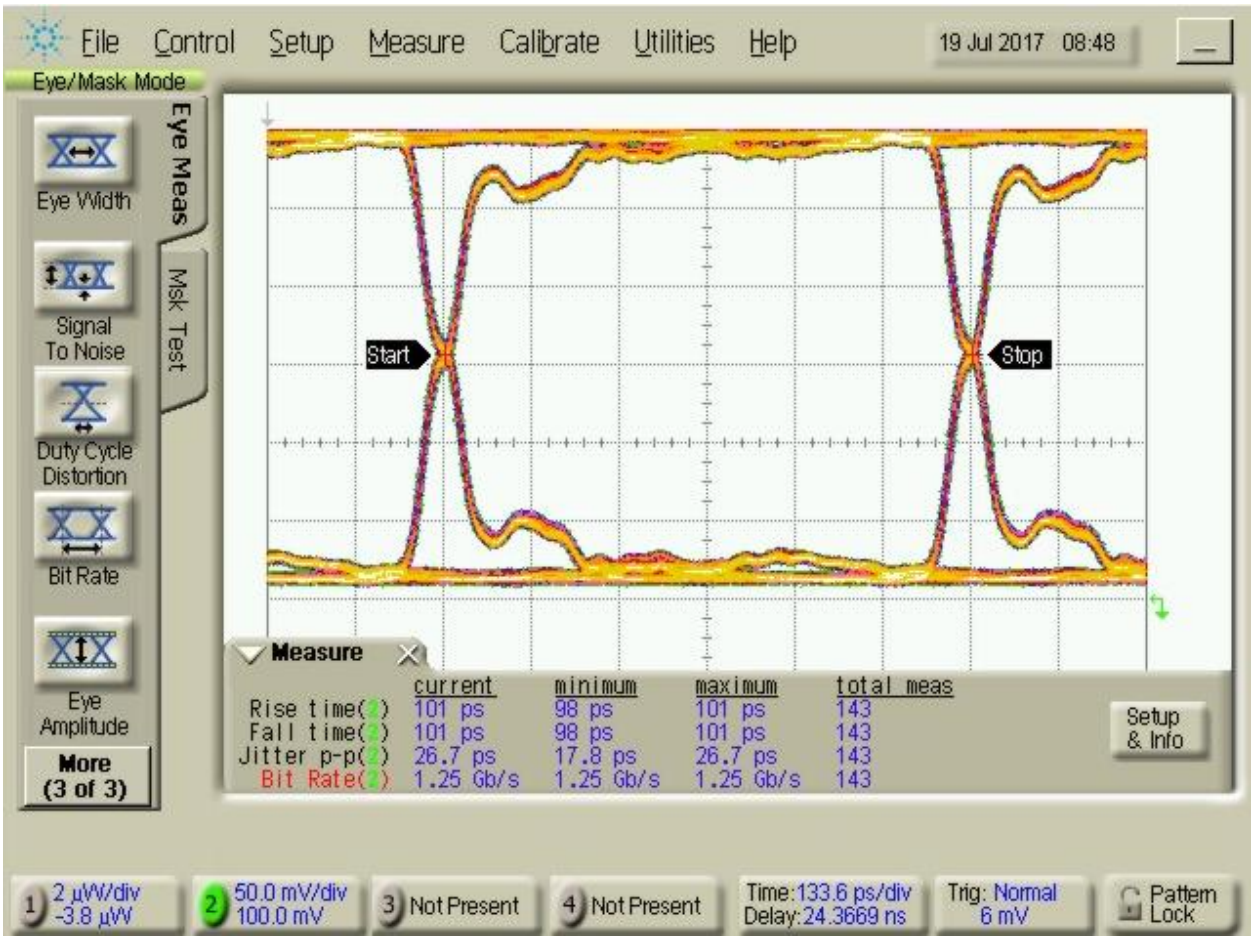


Figure 7: Eye diagram of GSSG configuration at 1.25Gbps

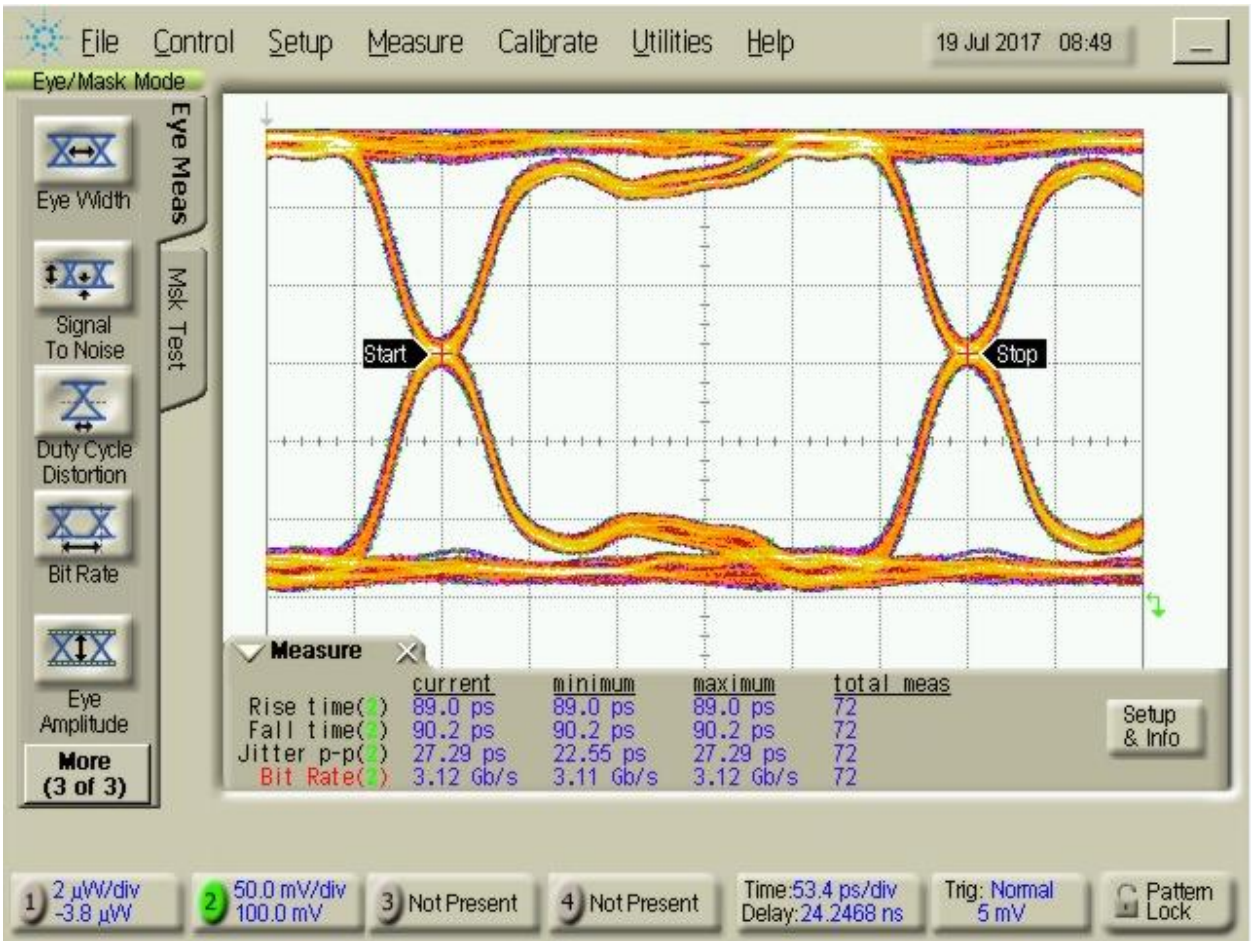


Figure 8: Eye diagram of GSSG configuration at 3.125Gbps

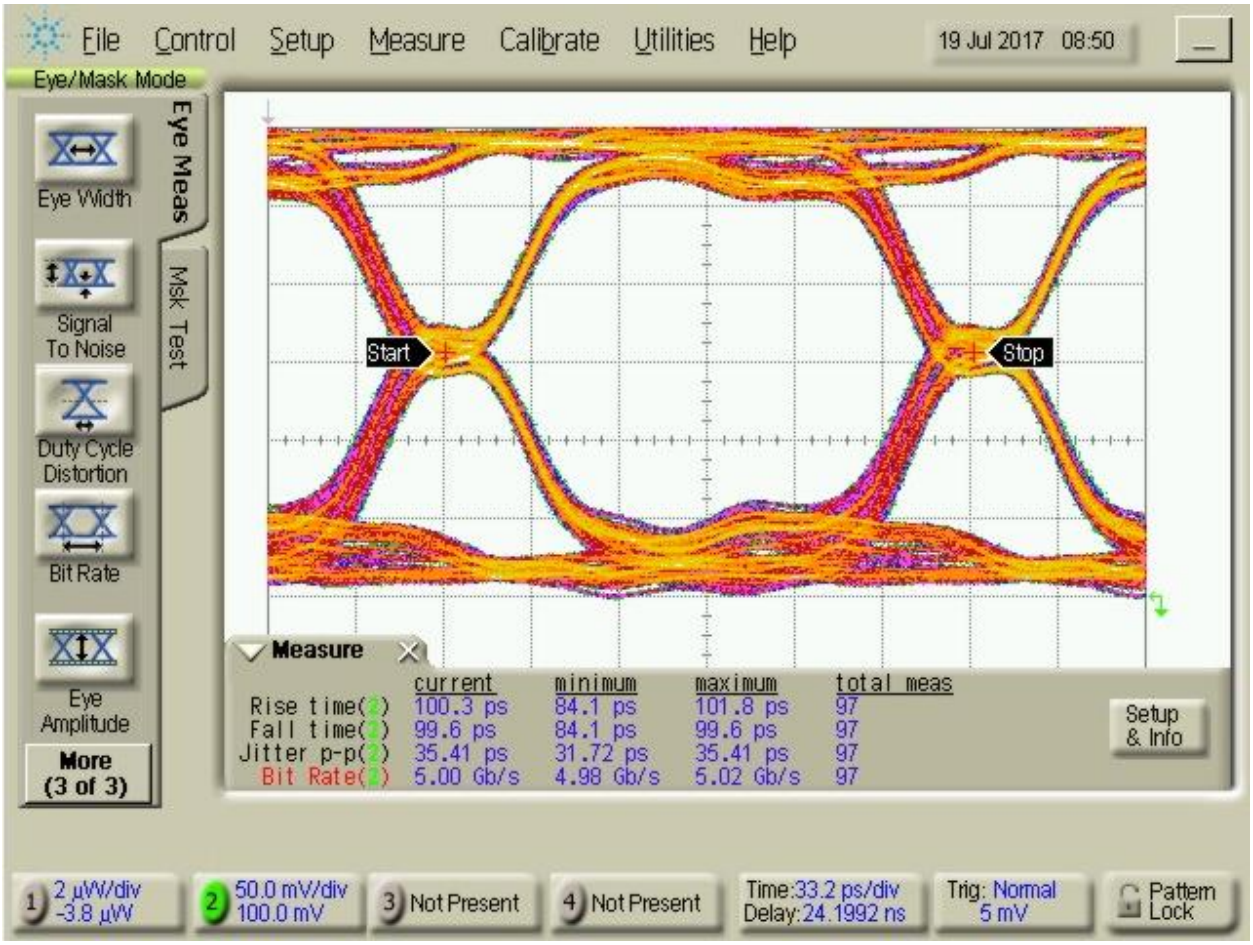


Figure 9: Eye diagram of GSSG configuration at 5Gbps

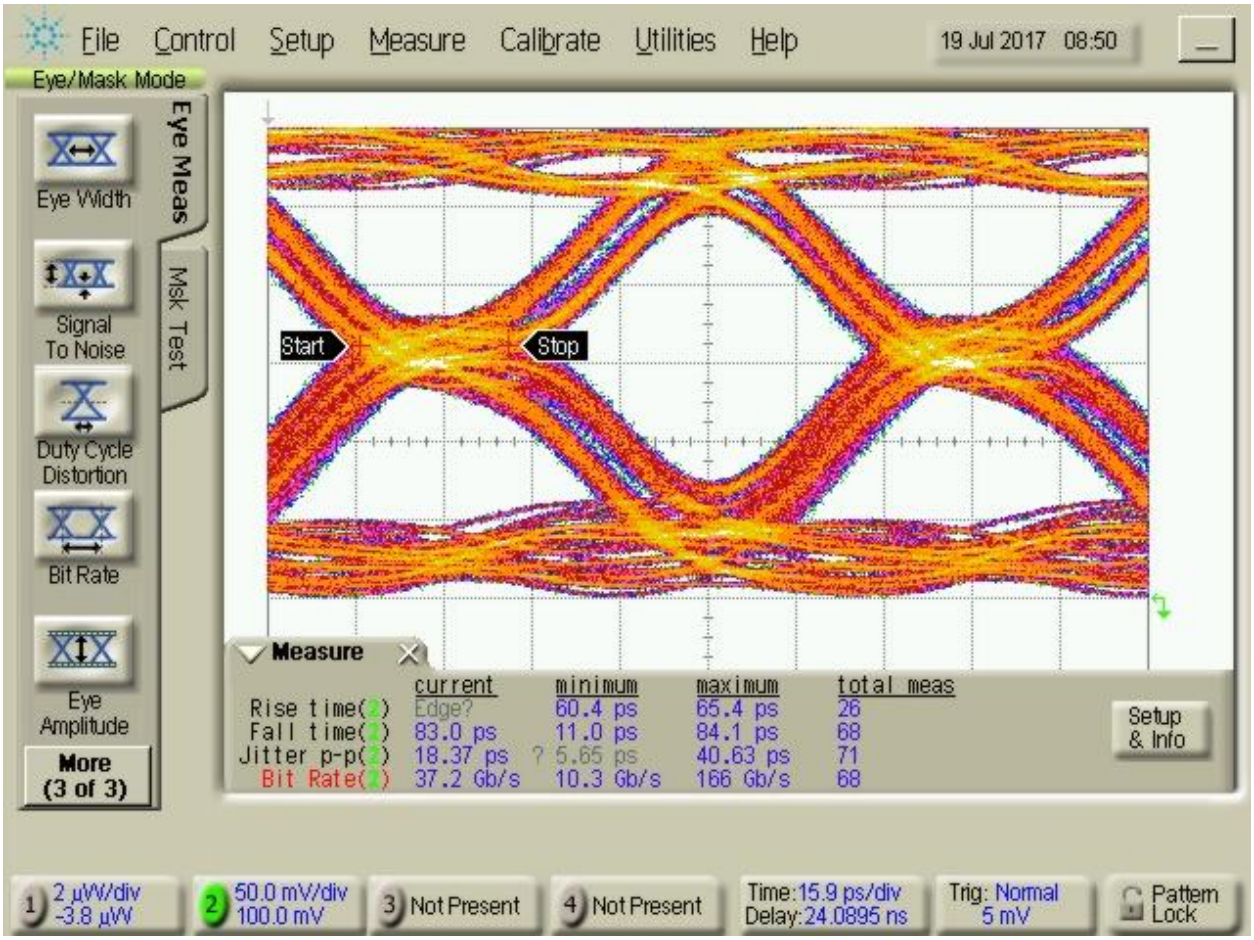


Figure 10: Eye diagram of GSSG configuration at 10.3125Gbps

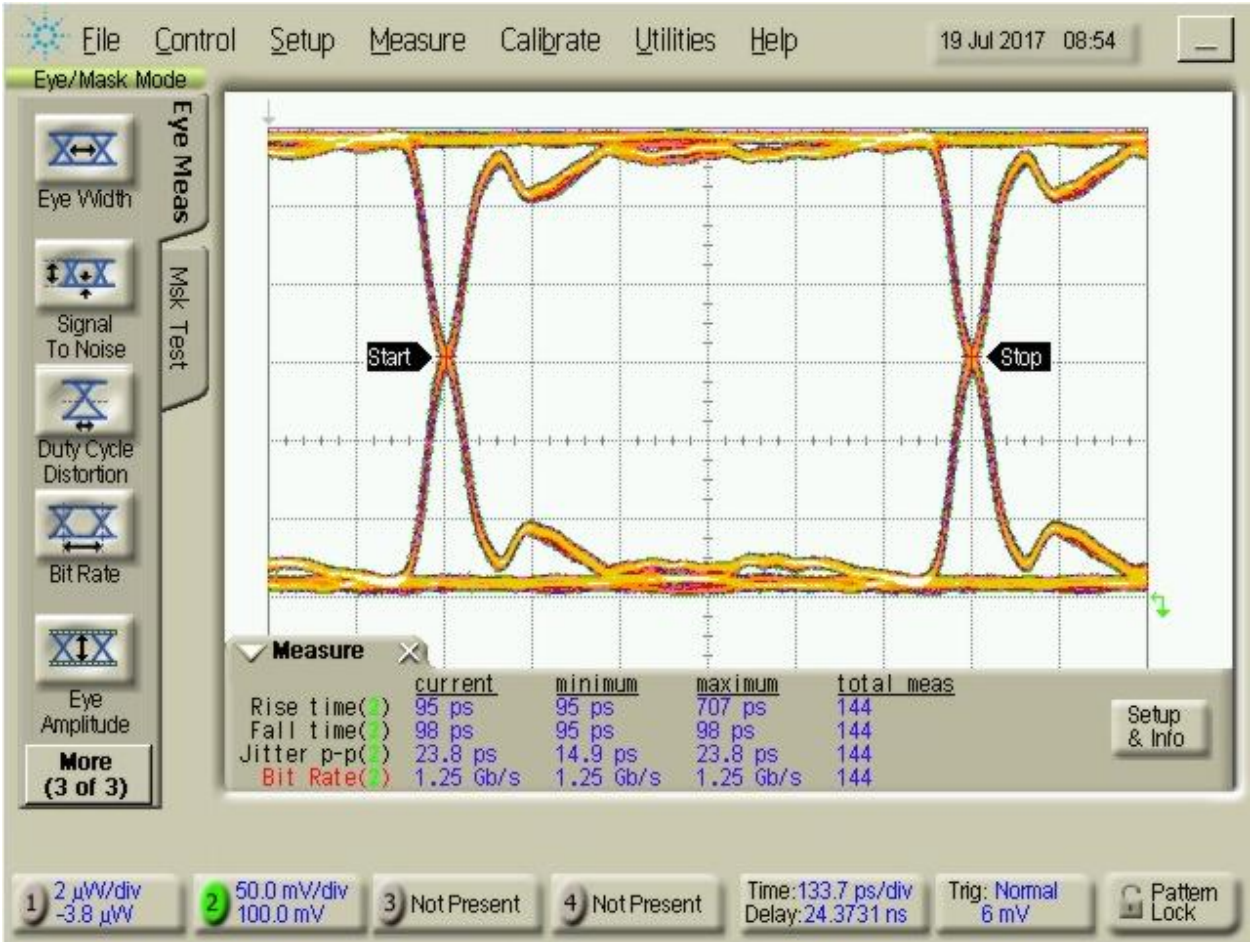


Figure 11: Eye diagram of DGSSG configuration at 1.25Gbps

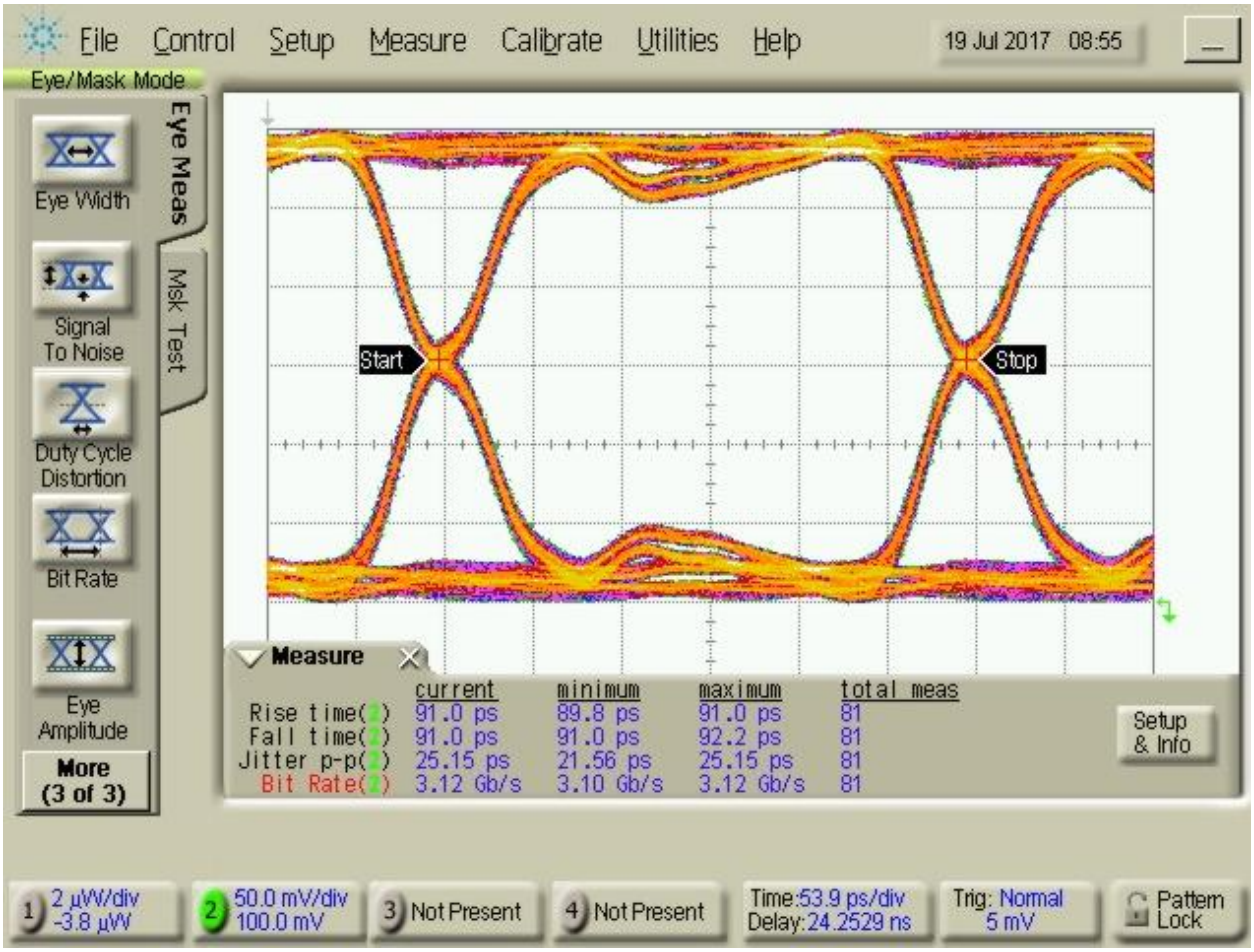


Figure 12: Eye diagram of DGSSG configuration at 3.125Gbps

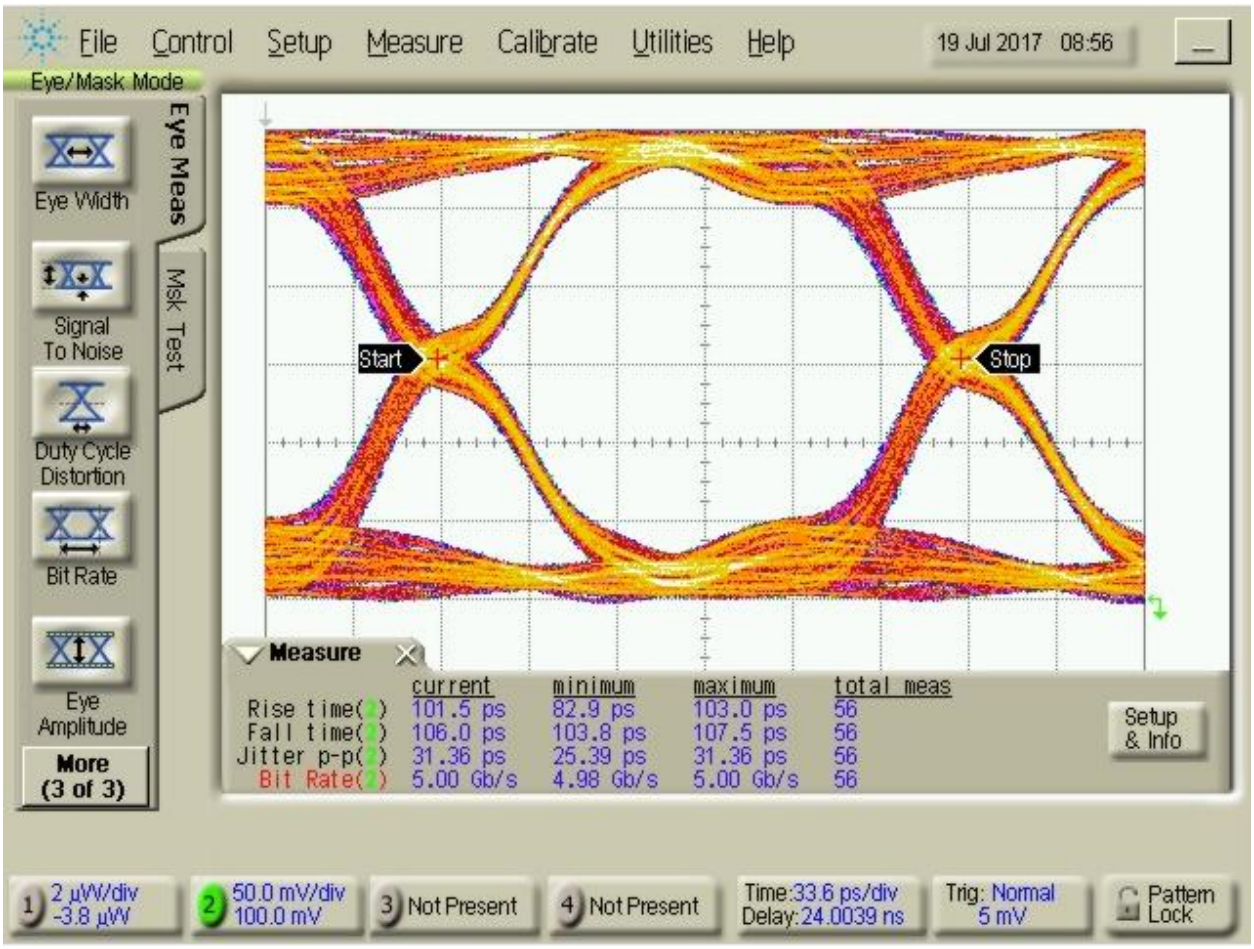


Figure 13: Eye diagram of DGSSG configuration at 5Gbps

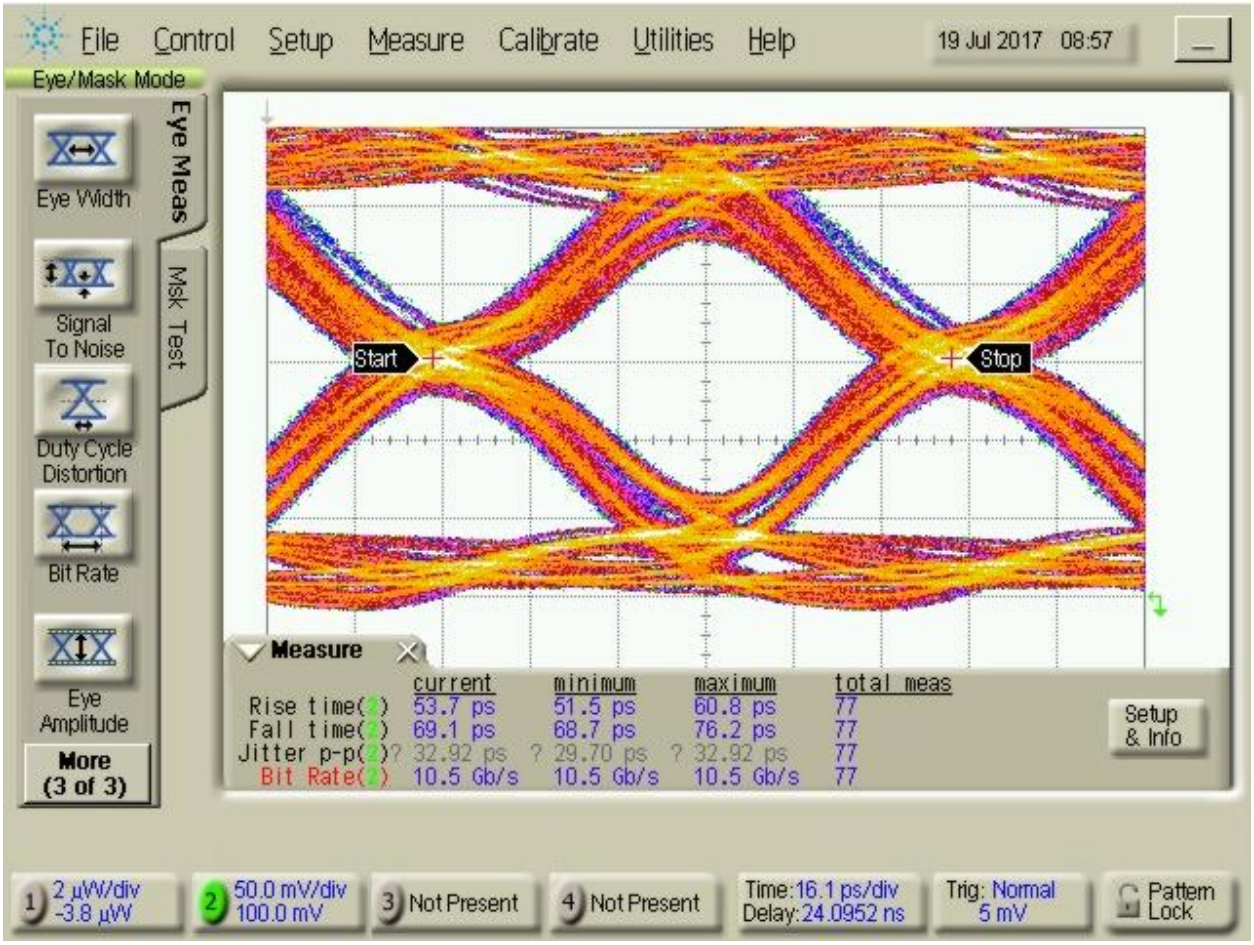


Figure 14: Eye diagram of DGSSG configuration at 10.3125Gbps

APPENDIX A – Test System Description

A test fixture printed circuit board was designed specifically for this analysis. All traces to the HD Stacker Connector contacts were designed to a nominal 50Ω ± 5% single-ended impedance but used in differential 100Ω pairs.

All tests were performed using the Agilent E5071C ENA network analyzer with option TDR. All frequency domain data (IL, RL, NEXT, FEXT) has a 2% smoothing filter applied within the network analyzer.

Test fixture and test cables were connected to the Agilent E5071C ENA Network Analyzer via high-performance 50-ohm coaxial test cables with SMA connectors. The system configuration is shown in the block diagram below:

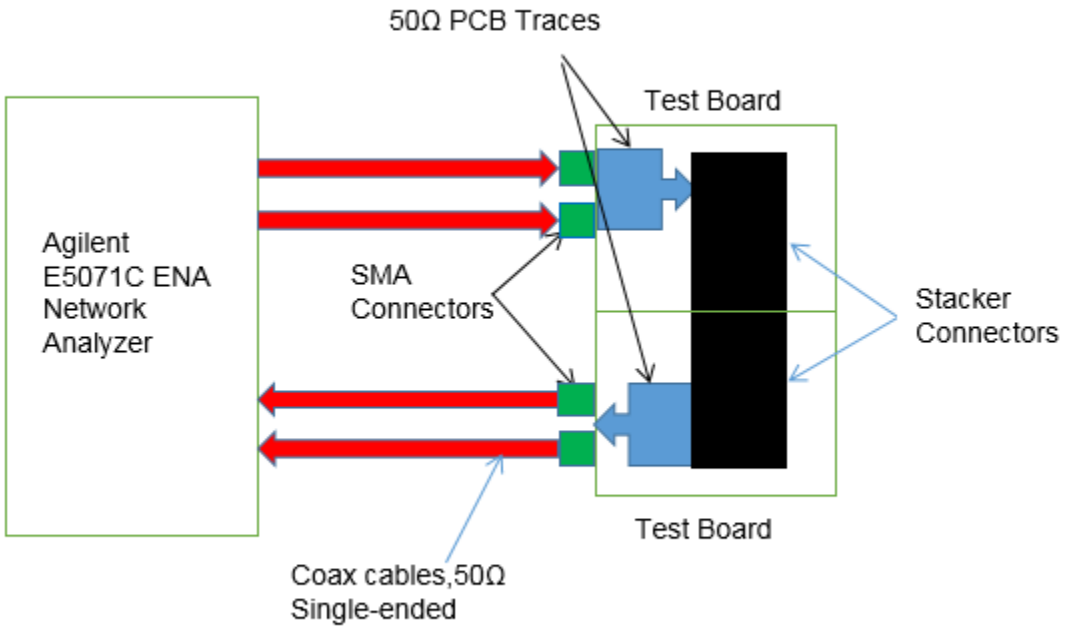


Figure 6: Test System Block Diagram

APPENDIX B – Data Acquisition Methods

Frequency Domain (S-Parameter) Procedures

To ensure precise and repeatable data acquisition, extreme care was taken in the test fixture design along with the calibration and testing procedure. A full calibration from 300kHz to 20GHz was performed prior to testing using the Agilent N4433A eCal module. After calibration, test leads were connected to the test fixture and applicable data was observed and saved into a .csv file. At the completion of testing the acquired data was loaded into spreadsheet and .S4p format for analysis and figure generation.

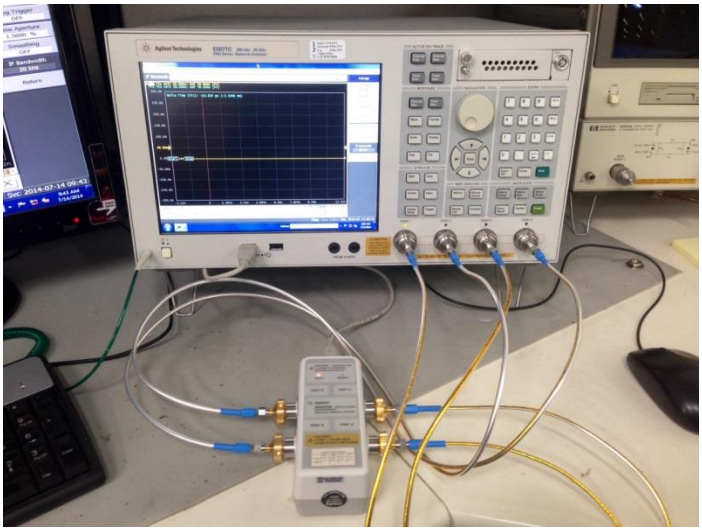
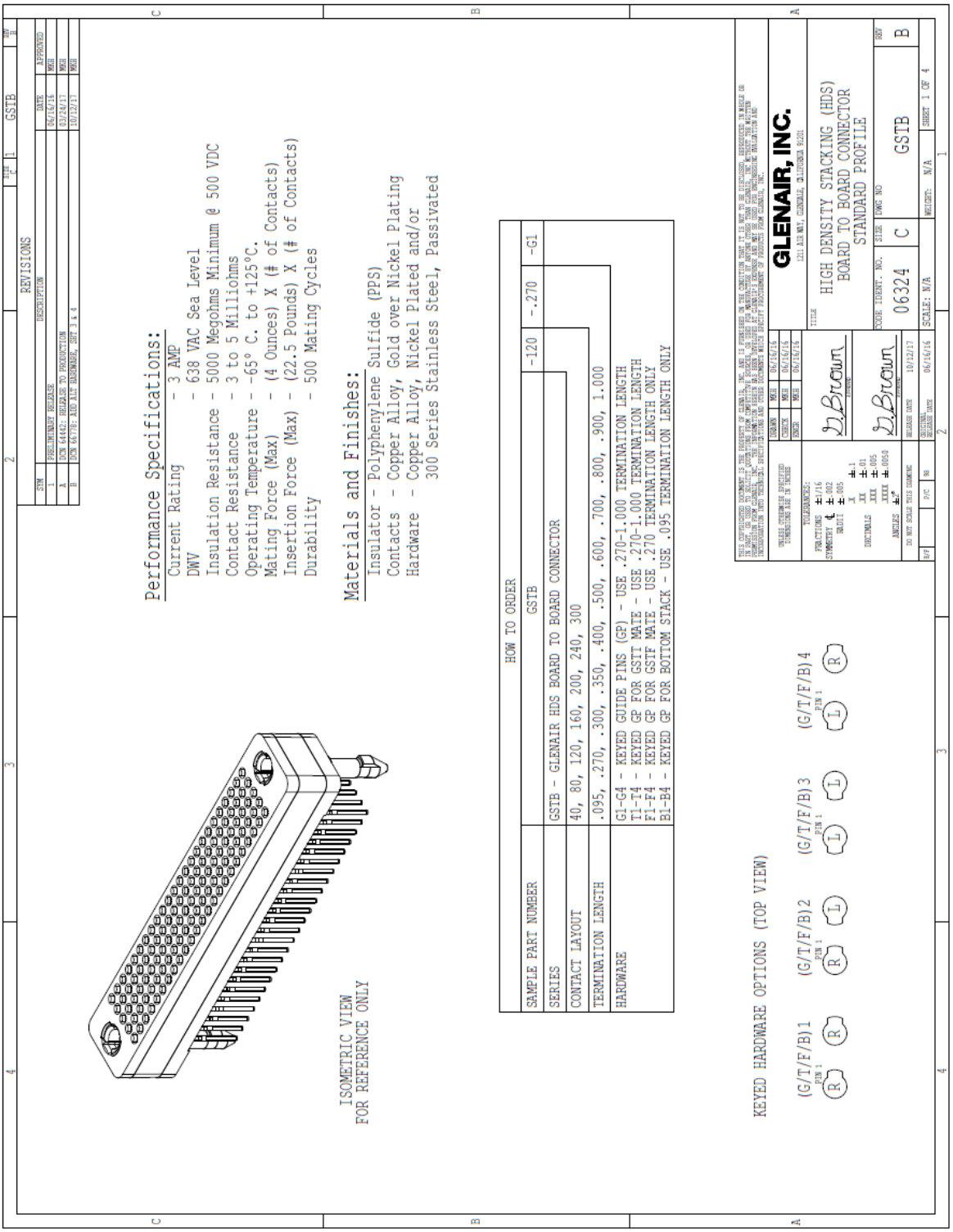


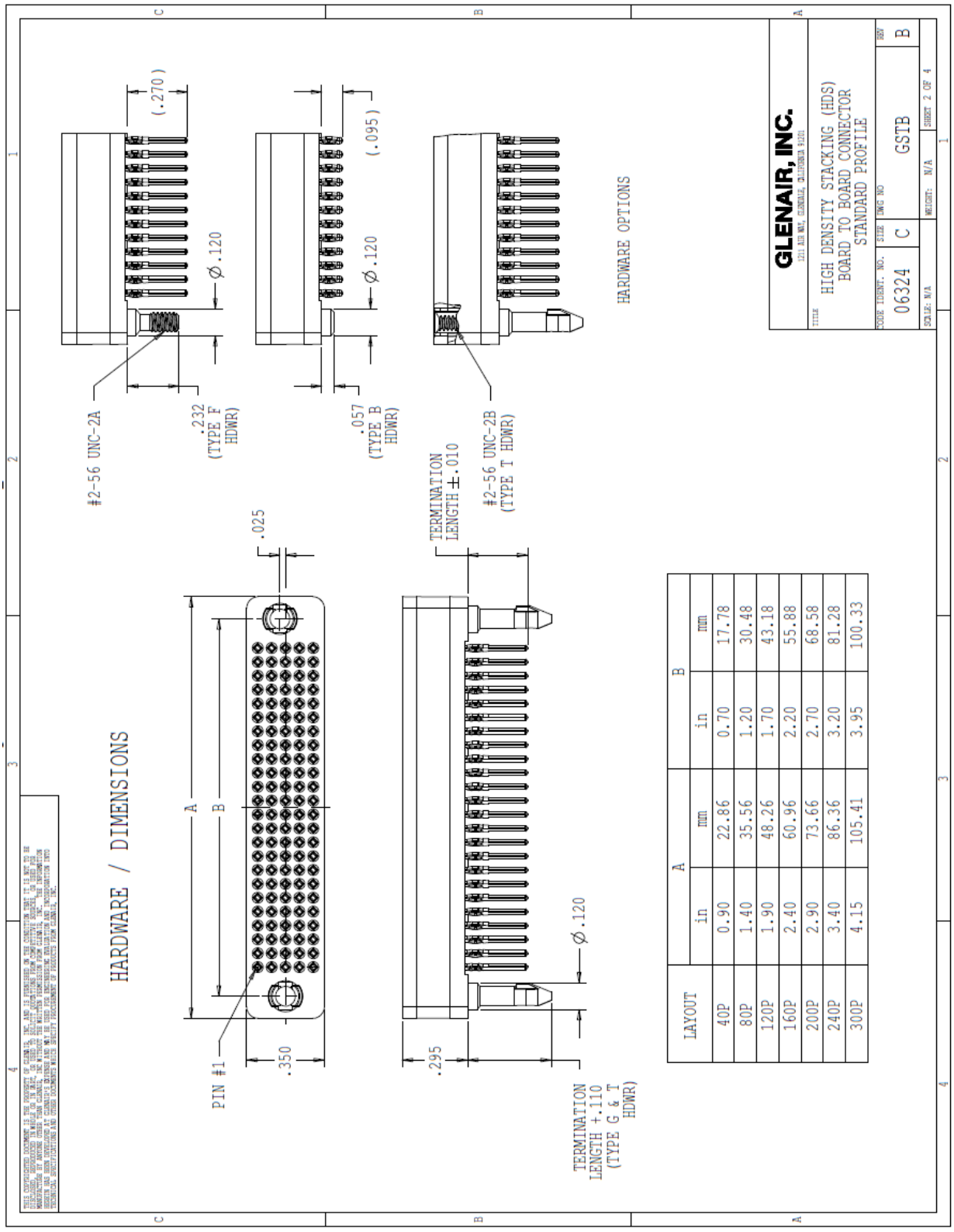
Figure 4: Network analyzer with eCal module

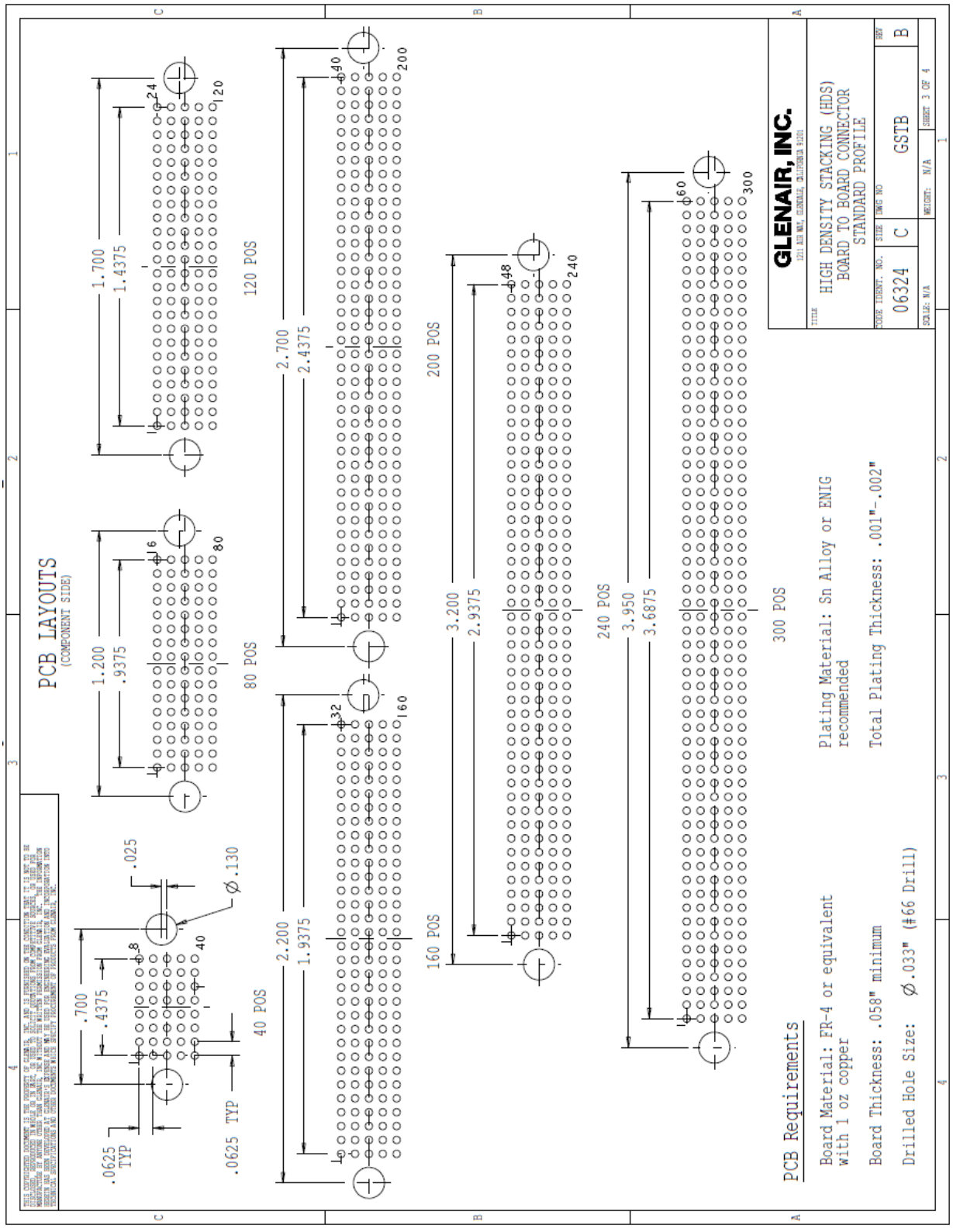
Time Domain Procedures

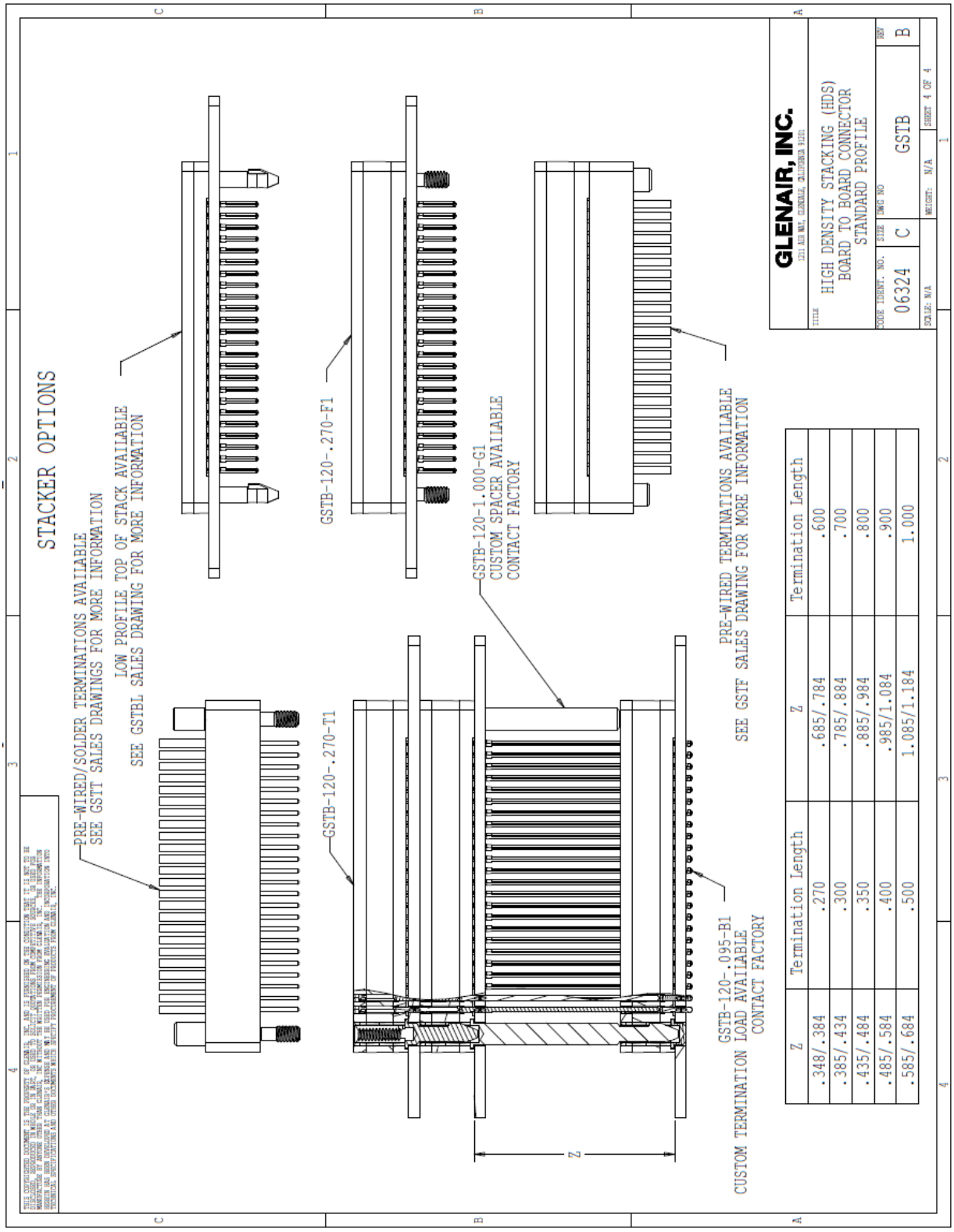
Historically, dedicated TDR equipment was necessary to analyze time-domain response of RF systems. The Agilent 5071C used for this testing contains software package “option TDR” which mathematically derives time-domain information from acquired frequency domain data (S-parameters). Even with bandwidth-limited data and a finite number of sample points, option TDR offers a very accurate TDR representation. In this report, the relationship between risetime and bandwidth was determined by using Time X Bandwidth = 0.446, an equation provided by Agilent for use with the 5071C.

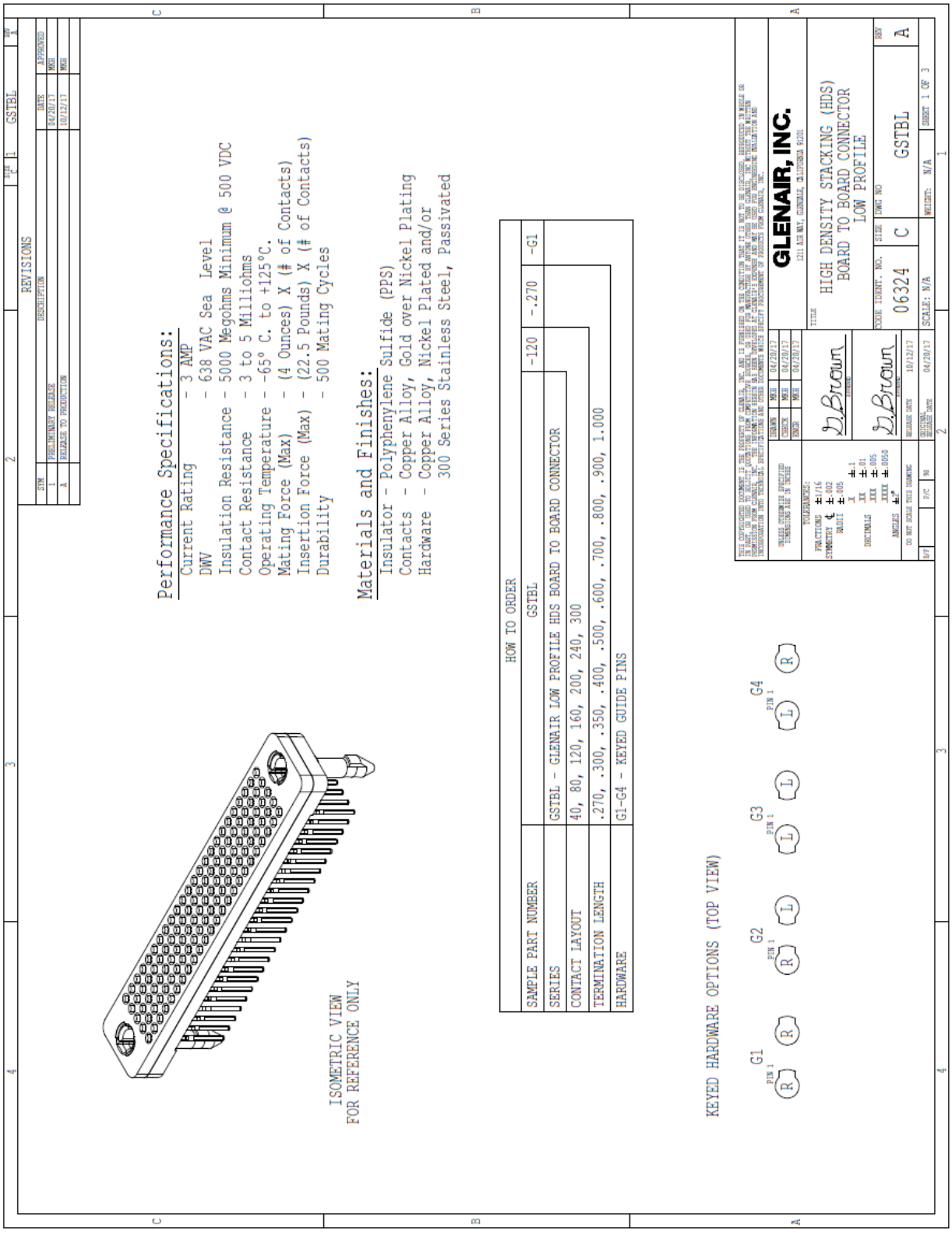
APPENDIX C – Applicable Drawings

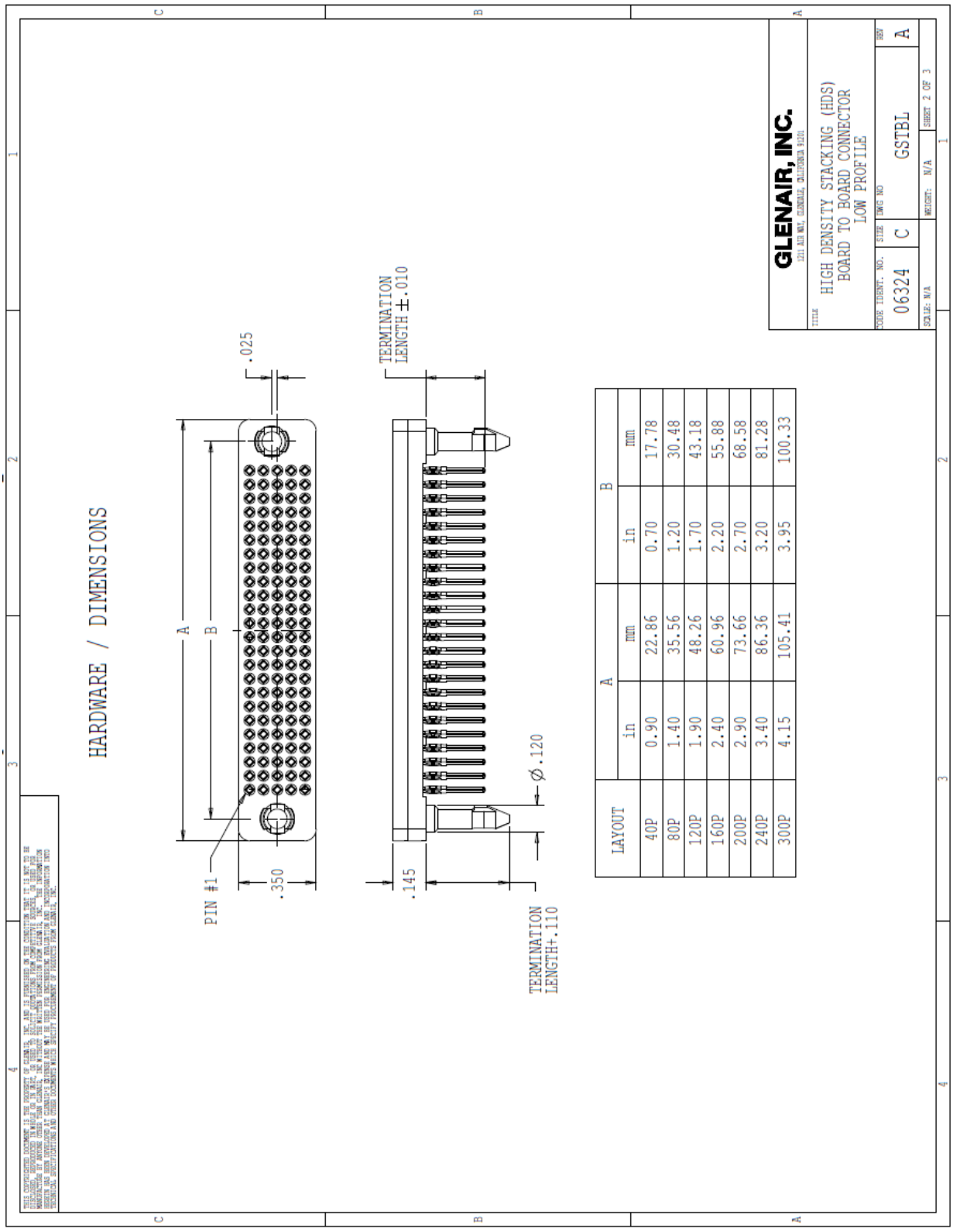




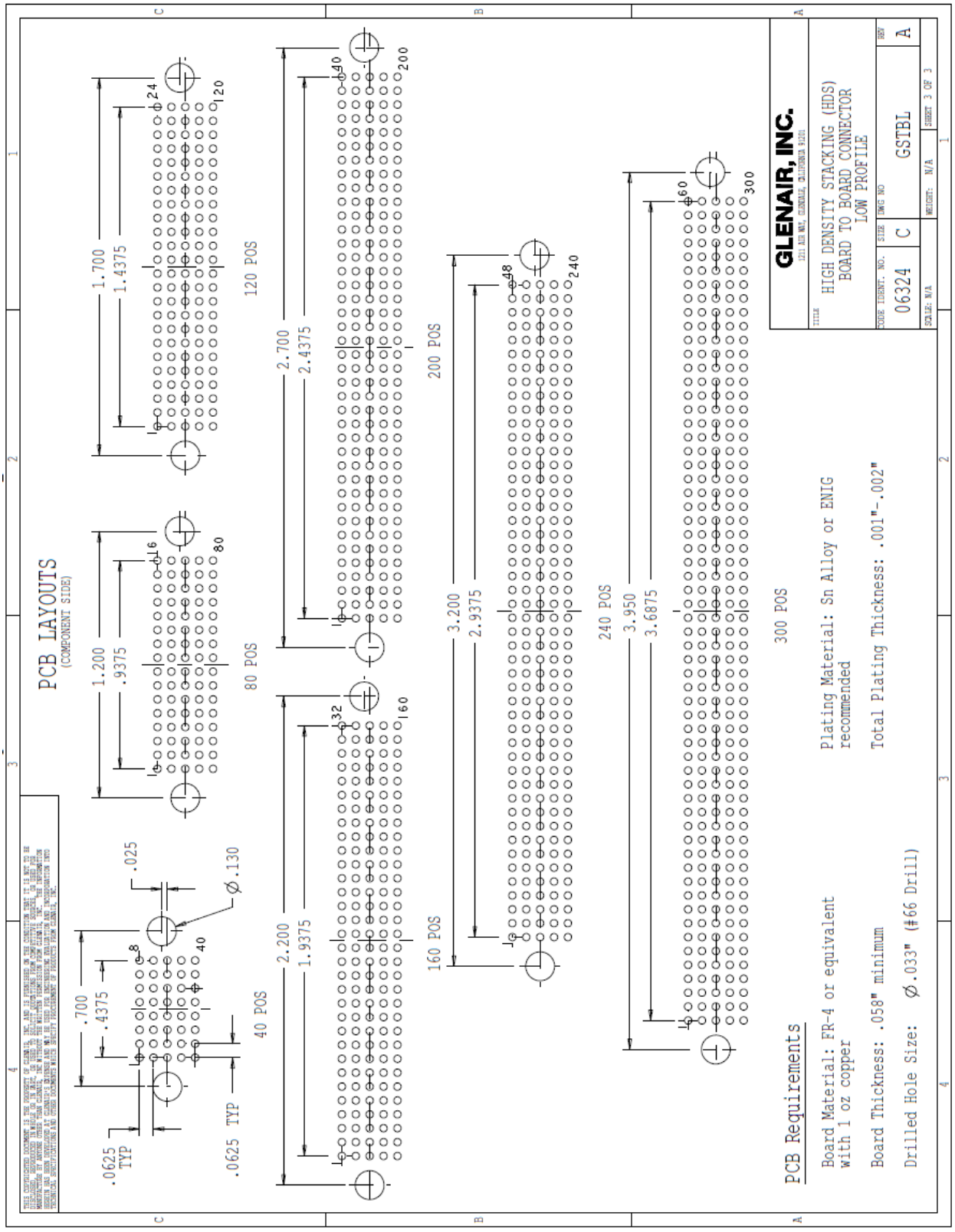



STACKER OPTIONS
PRE-WIRED/SOLDER TERMINATIONS AVAILABLE
SEE GSTT SALES DRAWINGS FOR MORE INFORMATION
LOW PROFILE TOP OF STACK AVAILABLE
SEE GSTBL SALES DRAWING FOR MORE INFORMATION
GSTB-120-.270-F1
GSTB-120-1.000-G1
CUSTOM SPACER AVAILABLE
CONTACT FACTORY
PRE-WIRED TERMINATIONS AVAILABLE
SEE GSTF SALES DRAWING FOR MORE INFORMATION
GSTB-120-.270-T1
GSTB-120-.095-B1
CUSTOM TERMINATION LOAD AVAILABLE
CONTACT FACTORY
Z
Z | Termination Length
.348/.384 | .270
.385/.434 | .300
.435/.484 | .350
.485/.584 | .400
.585/.684 | .500
Z | Termination Length
.685/.784 | .600
.785/.884 | .700
.885/.984 | .800
.985/1.084 | .900
1.085/1.184 | 1.000
GLENAIR, INC.
1211 AIR WAY, GLENDALE, CALIFORNIA 91201
TITLE
HIGH DENSITY STACKING (HDS)
BOARD TO BOARD CONNECTOR
STANDARD PROFILE
CODE IDENT. NO. 06324
SIZE C
DWG NO GSTB
REV B
SCALE: N/A
WEIGHT: N/A
SHEET 4 OF 4


REVISIONS
DESCRIPTION
PRELIMINARY RELEASE
RELEASE TO PRODUCTION
Performance Specifications:
Current Rating - 3 AMP
DWV - 638 VAC Sea Level
Insulation Resistance - 5000 Megohms Minimum @ 500 VDC
Contact Resistance - 3 to 5 Milliohms
Operating Temperature - -65° C. to +125°C.
Mating Force (Max) - (4 Ounces) X (# of Contacts)
Insertion Force (Max) - (22.5 Pounds) X (# of Contacts)
Durability - 500 Mating Cycles
Materials and Finishes:
Insulator - Polyphenylene Sulfide (PPS)
Contacts - Copper Alloy, Gold over Nickel Plating
Hardware - Copper Alloy, Nickel Plated and/or
300 Series Stainless Steel, Passivated
ISOMETRIC VIEW
FOR REFERENCE ONLY
HOW TO ORDER
SAMPLE PART NUMBER
GSTBL
-120
-.270
-G1
SERIES
GSTBL - GLENAIR LOW PROFILE HDS BOARD TO BOARD CONNECTOR
CONTACT LAYOUT
40, 80, 120, 160, 200, 240, 300
TERMINATION LENGTH
.270, .300, .350, .400, .500, .600, .700, .800, .900, 1.000
HARDWARE
G1-G4 - KEYED GUIDE PINS
KEYED HARDWARE OPTIONS (TOP VIEW)
G1
G2
G3
G4
PIN 1
GLENAIR, INC.
1211 AIR WAY, GLENDALE, CALIFORNIA 91201
HIGH DENSITY STACKING (HDS)
BOARD TO BOARD CONNECTOR
LOW PROFILE
GSTBL
06324
C
A
SCALE: N/A
SHEET 1 OF 3



LAYOUT	A		B	
	in	mm	in	mm
40P	0.90	22.86	0.70	17.78
80P	1.40	35.56	1.20	30.48
120P	1.90	48.26	1.70	43.18
160P	2.40	60.96	2.20	55.88
200P	2.90	73.66	2.70	68.58
240P	3.40	86.36	3.20	81.28
300P	4.15	105.41	3.95	100.33



APPENDIX D – HD Stacker Connector PCB Layout Guidelines

Pad Geometry

The HD Stacker Connector is designed for 29 mil pressed-fit holes on a 62.5 mil grid. A representative PCB footprint is found in Figure D1. PCB footprint layouts for each connector pin count can be found in the engineering drawings (Glenair document numbers GTSB and GTSBL).

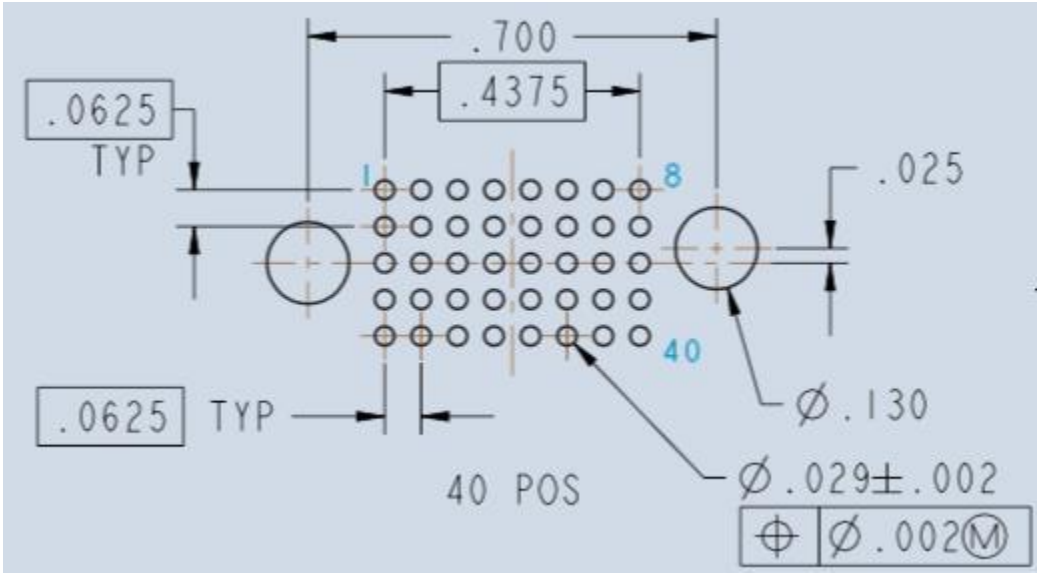


Figure D1. PCB Footprint for the 40 pin HD Stacker Connector.

The press fit hole should have a finished size of 29 mil ±2 mil. This can be achieved by using a #66 drill bit (33 mil) and plating with 1 mil minimum copper (with a tin alloy or ENIG finish). An 8 mil annular ring is recommended which will result in an overall pad diameter of 44 mil. An antipad with a diameter of 80 mils is also recommended. The pad geometry is summarized in Figure D2.

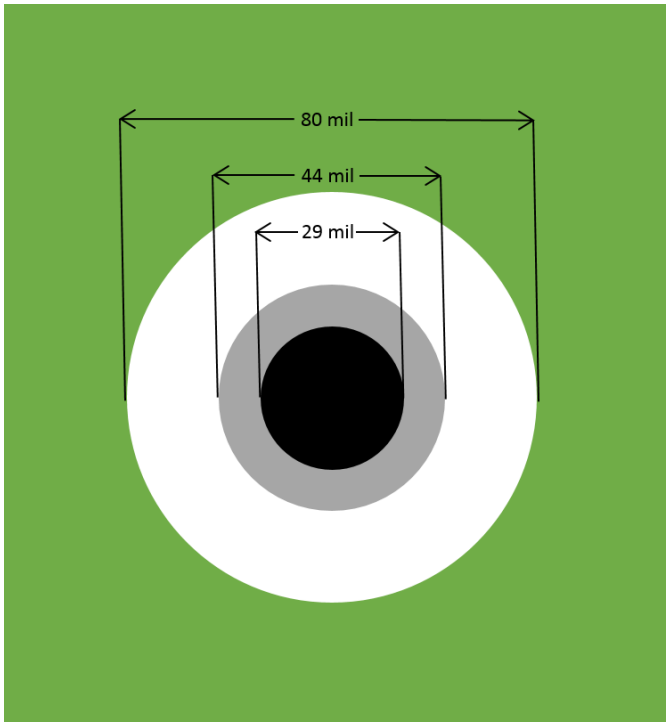


Figure D2. HD Stacker PCB Pad Geometry

Trace Geometry

PCB trace geometry for inner rows is constrained by pin pitch, hole geometry, and PCB manufacturer fabrication abilities. The maximum recommended escape trace width for inner connector rows is 9 mils. Pin spacing and annular ring size impose single ended, non-coupled routing from inner rows. The differential traces can be coupled after exiting the pin field. Figure D3 depicts differential pair escape routing which maximizes crosstalk isolation. Figure D4 shows an alternate escape routing scheme which increases the signal density at the sake of crosstalk isolation. Hybrid routing schemes between the two extremes can be utilized to meet an application's density and crosstalk requirements.

Traces should be routed on the PCB side opposite of the connector to minimize reflections caused by pin stubs.

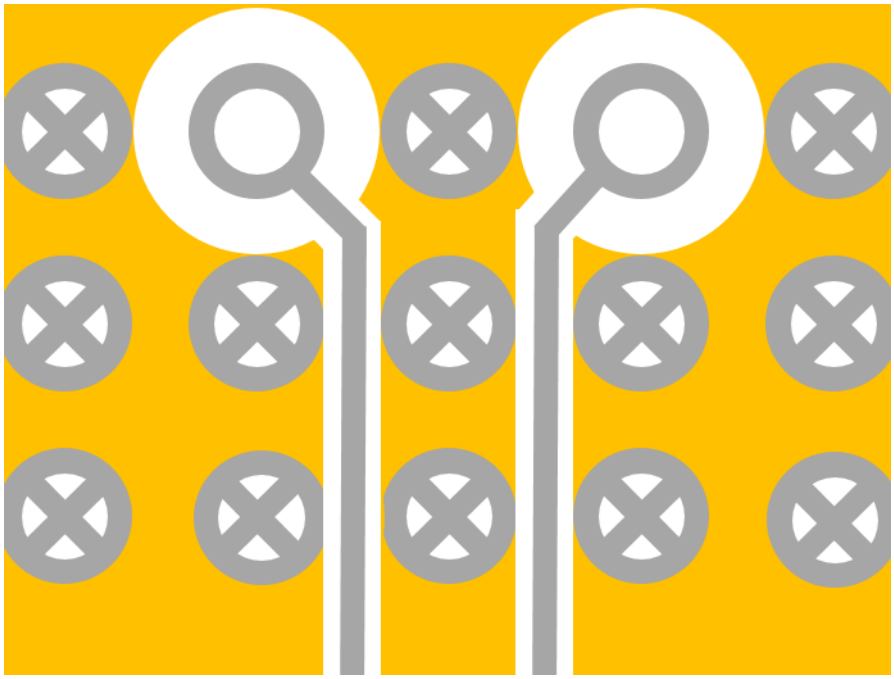


Figure D3. Inner Row Escape Routing

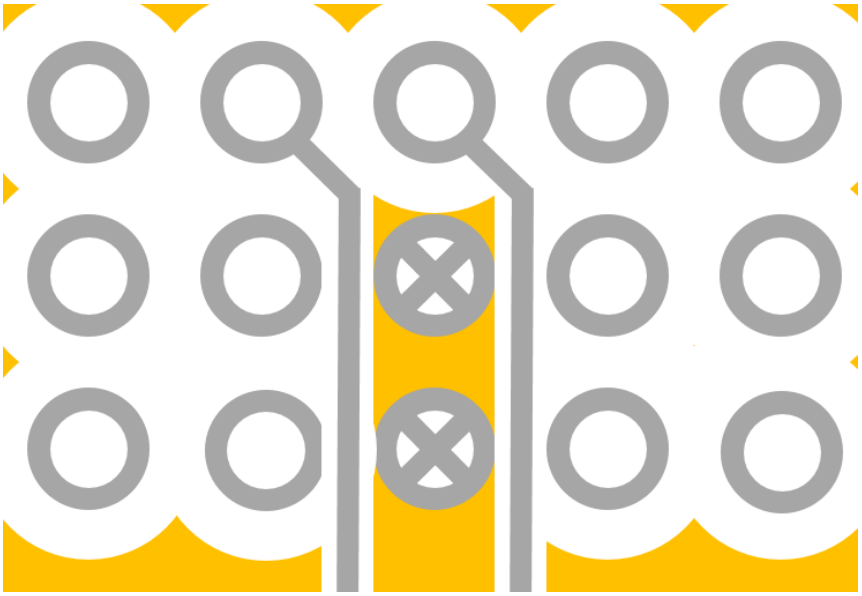


Figure D4. Alternate Inner Row Escape Routing

APPENDIX F - Glossary of Terms

DUT – Device under Test
FD – Frequency Domain
FEXT – Far-end Crosstalk
NEXT – Near-end Crosstalk
PCB – Printed Circuit Board
RF – Radio Frequency
RL – Return Loss
SE – Single-ended transmission
SI – Signal Integrity
SUT – System under Test
TD – Time Domain
TDA – Time Domain Analysis
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
VSWR – Voltage Standing Wave Ratio
Z – Impedance (Ω)